VIDEO-BANDWIDTH ENHANCEMENT OF RF POWER TRANSISTORS THROUGH VOLTERRA ANALYSIS

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VIDEO-BANDWIDTH ENHANCEMENT OF RF POWER TRANSISTORS THROUGH VOLTERRA ANALYSIS

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To my family :

Mom, Dad, Zeeshan and Anisha

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Research projects typically have a few authors, but it takes contributions, however small, from many individuals who contribute to their success. I would like to extend my earnest acknowledgements to all individuals who have contributed to this research.

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SUMMARY

The signal bandwidth requirements for Base Station RF Power Amplifiers has increased with the advent of multicarrier systems employing carrier aggregation. RF pre-matching of high power transistors involves considerations of impedance matching, RF bandwidth, phase characteristics as well as physical realization. Due to their large-area topologies, the high capacitance of the power transistors used in high-power PAs inherently limits their bandwidth. One of the reasons for this limitation is the presence of sharp resonances in the bias networks of the power amplifier at modulation frequencies. Due to this increase in signal bandwidth requirements of next generation applications, it has become necessary to incorporate circuits that address the low frequency baseband impedance to ensure the power transistor is capable of amplifying these signals with minimum distortion as well as correct within specifications using digital predistortion systems. In this research, we analyze the baseband response of a widely used pre matching topology for RF Power Transistors as well as propose and analyze modifications that allow for improved large signal bandwidth operation. The results show than an ACLR improvement of approximately 10dB resulted from the addition of an integrated bias network with damping resistance that feeds the drain using the same DPD complexity. Integrating the bias network into the same package as the power transistors is the novel innovation that allows for this improved ACLR. We also demonstrate the signal bandwidth limitations of current RF power amplifiers, propose and analyze the methodology used to improve this capability and demonstrate its application in a high power asymmetric Doherty PA. The designed Doherty Power Amplifier achieves 56dBm of peak power from 1.805-1.88GHz with 50% efficiency at 8dB backoff from peak power. The circuit demonstrates >200MHz

of video-bandwidth (two-tone onset of resonance) and improved DPD correction for a multi-Carrier multi-Standard signal, thus achieving the best combination of output power, efficiency and linearity reported to date.

CHAPTER I

INTRODUCTION

Radio Frequency (RF) Power Amplifiers (PA) perform an important function in any communication system. They are responsible for increasing the power level of the signal before it is transmitted through an antenna.

The RF Power Transistor is the workhorse of any PA sub-system. It is responsible for converting the low-level modulated signal to its amplified version by taking advantage of the transconductive properties of its active device.

The main components of any power transistor are the active die (for example laterally diffused metal-oxide semiconductor (LDMOS) or gallium nitride (GaN) transistors) as well as integrated or discrete passive components. These passive components function as matching elements to transform the typically low die impedances to levels that can be impedance matched using an interface such as a printed circuit board (PCB).

Communication systems are inherently limited in the signal bandwidth that they can process. These limitations can arise from baseband processing or at other points along the transmitter/receiver chain. RF Power transistors, by design, are limited in the signal bandwidth that they can amplify before they begin to incur severe levels of distortion. One of the sources of this distortion are varying impedance levels presented to the active device current source in the low frequency baseband modulation frequency range.

It is the purpose of this research to study the causes of this distortion and propose solutions to overcome this limitation of RF Power Transistors.

CHAPTER II

BACKGROUND INFORMATION

2.1 Device Technologies for High Power RF

Field effect transistors remain the technology of choice for high power RF applications. The structure of FETs is usually modified to meet the strenuous requirements of the end application. Two competing technologies for high power RF transistors are LDMOSFET (Laterally Diffused Metal-Oxide Semiconductor Field effect Transistor) and GaN HEMT (Gallium Nitride High Electron Mobility Transistor).

Figure 1 shows a two metal layer LDMOSFET device structure [1]. Some notable features of this structure are

- P+ Sinker : Connects the back side source contact to the intrinsic source. This region is heavily doped for low resistance and inductance to enable high frequency operation.

- N- Drift Region : This is a lightly doped region connected between the bottom of the gate and the highly doped drain contact and provides for high breakdown voltages, low on state resistance (RDSON) and Hot Carrier Injection Reliability.

- Metal1 + Metal2 Drain : Designed to meet electromigration specifications for high reliability.

- Metal-2 Gate Bus : This runs parallel to the intrinsic gate and makes periodic connections with the intrinsic gate to reduce its resistance.

- M1 Faraday Shield : This is an extension of the source metal over the gate to reduce feedback capacitance.

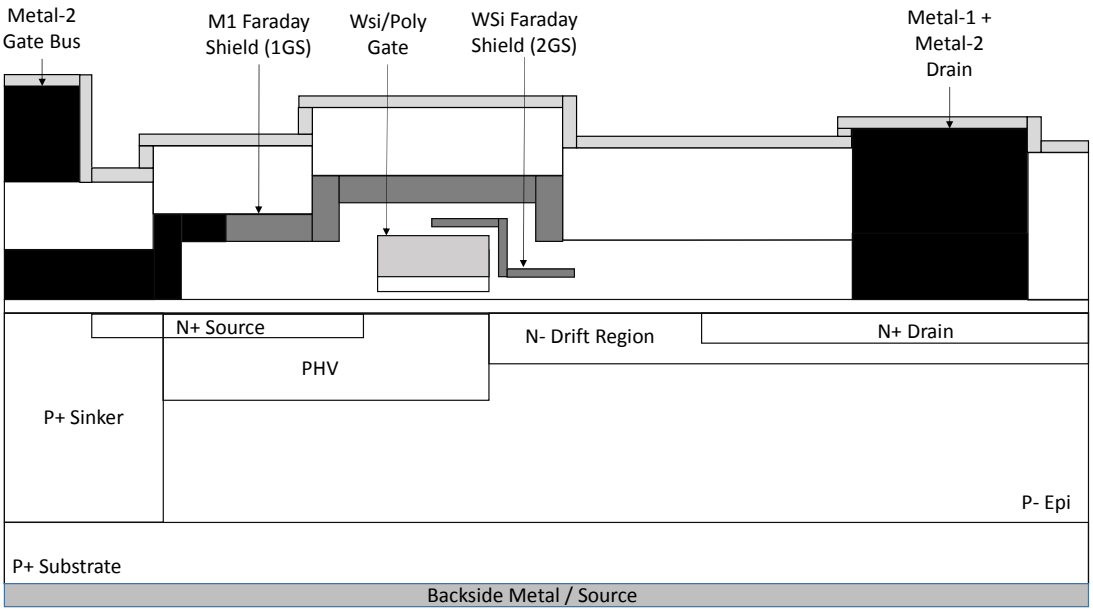

Figure 1: LDMOS Structure [1]

- WSi Faraday Shield : This is a thin, grounded WSi conductor between the gate and the drain metal. It acts to further reduce the feedback capacitance as well as to improve the surface potential to improve performance and reliability.

Figure 2 shows a two metal layer GaN HEMT device structure [2]. Some notable features of this structure are

- SiC Substrate : The Gallium Nitride epitaxial wafers are grown on Silicon Carbide (SiC) substrates using MOCVD (Metal Organic Chemical Vapor Deposition) process.

- Ti-Al based Ohmic Contacts : Ohmic Contact Resistances are typically 0.2-0.3 ohm-mm.

- Backmetal/Source : 10 micrometer thick plated Au is deposited on the backs of the wafers.

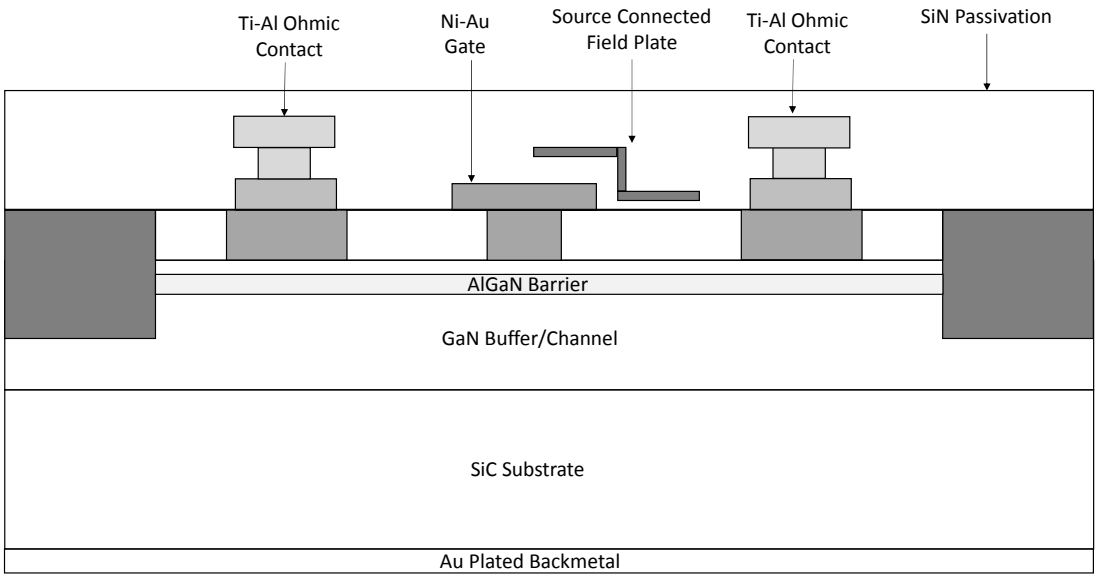

Figure 2: GaN Structure [2]

2.2 Johnson's Figure of Merit

The performance limit of a power transistor is set by the product

$$E * v_s/2\pi \tag{1}$$

where E is the electric field strength for dielectric breakdown and v_s is the minority carrier saturated drift velocity [3]. This product evaluates to $2 * 10^{11}$ for Silicon which indicates that a semiconductor material is capable of energizing the charges that process a signal. For high frequencies, only a small amount of energy can be imparted to a charge carrier due to the short time period. This results in lower power amplification. The converse is true for lower frequencies. Thus the device physics results in an inverse relationship between frequency and power parameters.

Figure 3 shows a comparison between Si, GaAs and GaN technologies [4]. In heterostructures, the discontinuity in the interface (AlGaN/GaN) leads to a significant sheet carrier concentration on the GaN side of the interface (Two-Dimensional

Electron Gas or 2DEG) . Saturation velocity of 2DEG carriers is an important design parameter for HEMTs, since it limits the maximum drain-source current achievable. Assuming that the electron loses all its kinetic energy gained from the field by emitting optical phonons, the time-averaged saturated drift-velocity is

$$v_{sat} = \frac{1}{2}\sqrt{\frac{\hbar\omega_{op}}{m^*}} \tag{2}$$

which yields $v_{sat} \approx 2x10^7$ cm/s. In Silicon, the carrier saturation velocity is limited by scattering mechanisms. However, in the case of a heterostructure 2DEG, the surface scattering is not that important and the impurity scattering is screened by a high density of electrons in the channel. This leads to a higher saturated velocity in heterostructures and hence a higher Johnson FOM.

Thus Gallium Nitride shows the highest potential for higher power and higher impedance devices for a given transition frequency.

Table 1 shows the values for band gap energy (E_g), breakdown electric field (E_{br}) and saturation drift velocity (v_{sat}) for GaN, GaAs and Si technologies [4].

Table 1: Technology Comparison

Material	E_g(eV)	E_{br}(MV/cm)	v_{sat}(cm/s)
Gallium Nitride	3.4	3.3	$2 * 10^7$
Gallium Arsenide	1.4	0.4	$1.8 * 10^7$
Silicon	1.1	0.3	$1 * 10^7$

In addition to avalanche breakdown, LDMOS power transistors exhibit a secondary breakdown phenomena known as Snapback. The LDMOS device structure inherently supports the formation of a parasitic bipolar transistor.For large sink currents, this bipolar transistor can be triggered and this can lead to a ruggedness failure. Optimization of the base resistance, gain and amplitude of the base current of the bipolar are critical to design a rugged LDMOS device [5] . A Transmission Line Pulse (TLP) measurement is used to characterize this snapback effect.

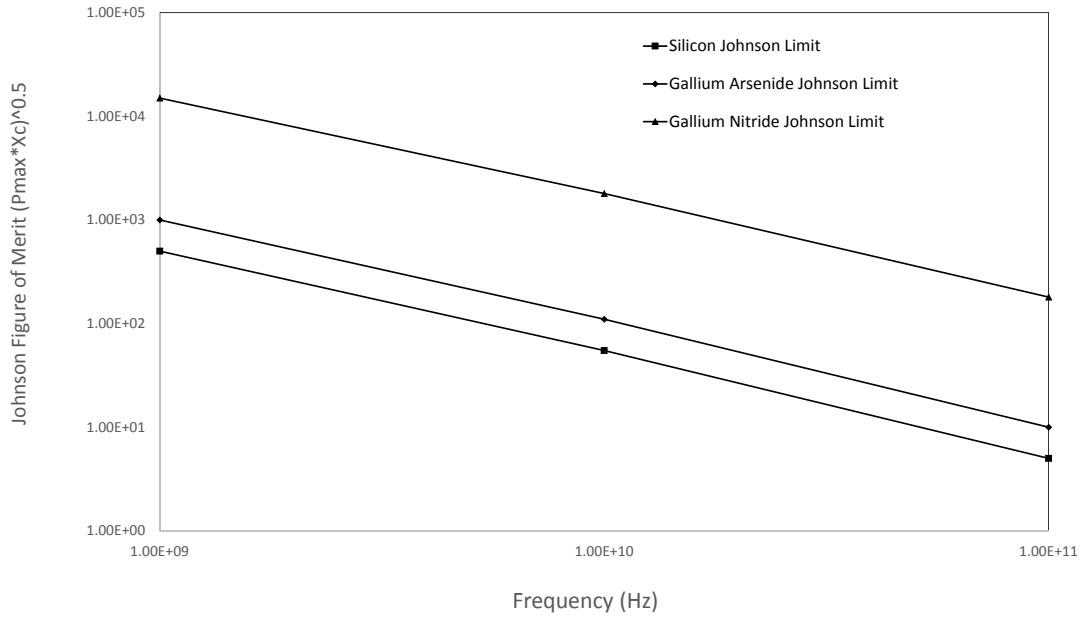

Figure 3: Comparison of the Johnson Figure of Merit for Si, GaAs and GaN technologies [4]

Current Crowding effects in Gallium Nitride based devices occurs due to material properties as well as geometric factors. Commonly, this is seen in GaN Mesa LED Structures due to the geometry of the device and the difference in conductivity between the n & p-type layers. Another case where current crowding commonly occurs is in strip lasers where the effect is almost purely due to the small contact size in relation to the rest of the device [6].

2.3 Types of Transistors

RF power transistors are designed in one of two main forms :

- Discrete Transistors
- Integrated Circuit Transistors

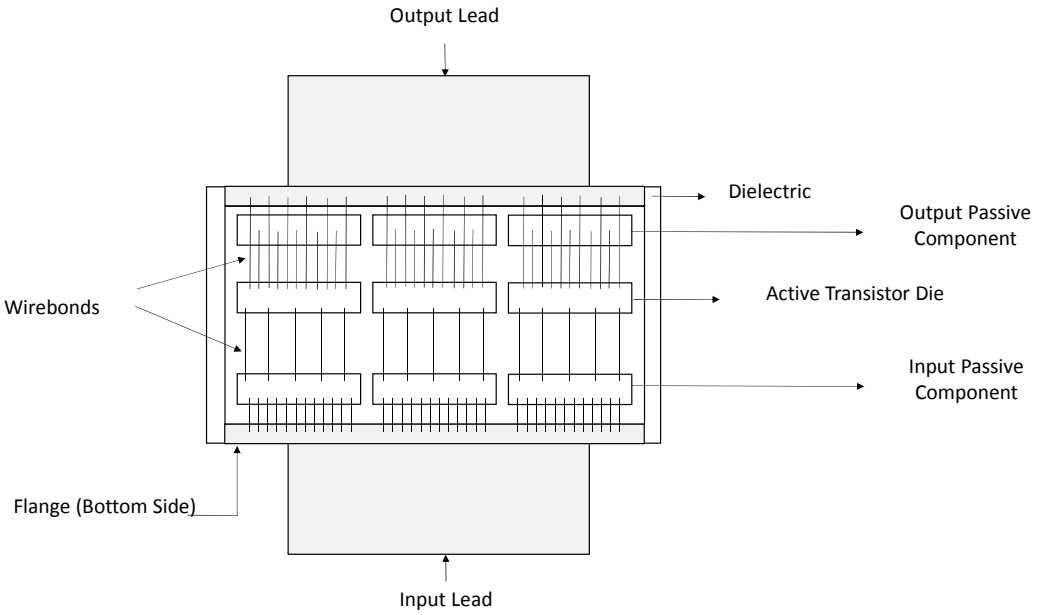

Figure 4: Discrete RF Power Transistor

Figure 4 shows an example of a Discrete RF Power Transistor. The main components of this type of transistor are:

- Input and Output Leads : Provide connections between the transistor die and the outside world. The leads typically make connections to some form of interface such as a Printed Circuit Board.

- Dielectric : The leads rest on some form of low loss dielectric. It forms an isolating layer between the lead and the flange (which is grounded). The dielectric thickness, material and lead geometry will determine the parasitic capacitance that is introduced by the lead.

- Input and Output Passive Components : These form portions of the input and output impedance matching networks that transform the typically low die level impedances to some higher value for ease of impedance matching. The passive components can be capacitors (series or shunt, for example Metal-Oxide

Semiconductor Capacitors OR Metal-Insulator-Metal Capacitors) or inductors (series or shunt, for example coil inductors on some substrate). The quality factors of these passive components will determine the insertion loss introduced by the matching networks as well as the total impedance transformation ratio from the die to the lead.

- Active Transistor Die : This represents the active device such as LDMOS or GaN FET. The physical dimensions of each die are determined by parameters such as Gate Periphery, Unit Gate Width and Drain-Source pitch.

- Flange : The flange forms the conductive substrate upon which the various die are bonded. The flange forms the source contact for the field effect transistor and is grounded in any application. The flange material plays an important role in heat dissipation as well as low-loss grounding. The materials used for the flange could be highly conductive metals such as gold or copper. The back-metal of the die are chosen to provide a very low coefficient of thermal expansion mismatch with the flange.

- Wirebonds : Wirebonds provide a mechanism to interconnect the various die and connect the die to the package lead. At RF and microwave frequencies, the self-inductance of these wirebonds plays a critical role in impedance matching. Wirebonds are typically designed for a particular shape and thus parameters such as wire radius, height and peak location are critical to any matching network design. The wirebonds are typically made out of low loss metals such as gold or aluminum. At high powers, any wirebond array should be capable of handling DC as well as AC currents reliably.

Figure 5 shows a block diagram for an example integrated power transistor [7]. Integrated Transistors differ from discrete transistors in the fact that they are monolithic in form. The active portion as well as the input, interstage and output matching

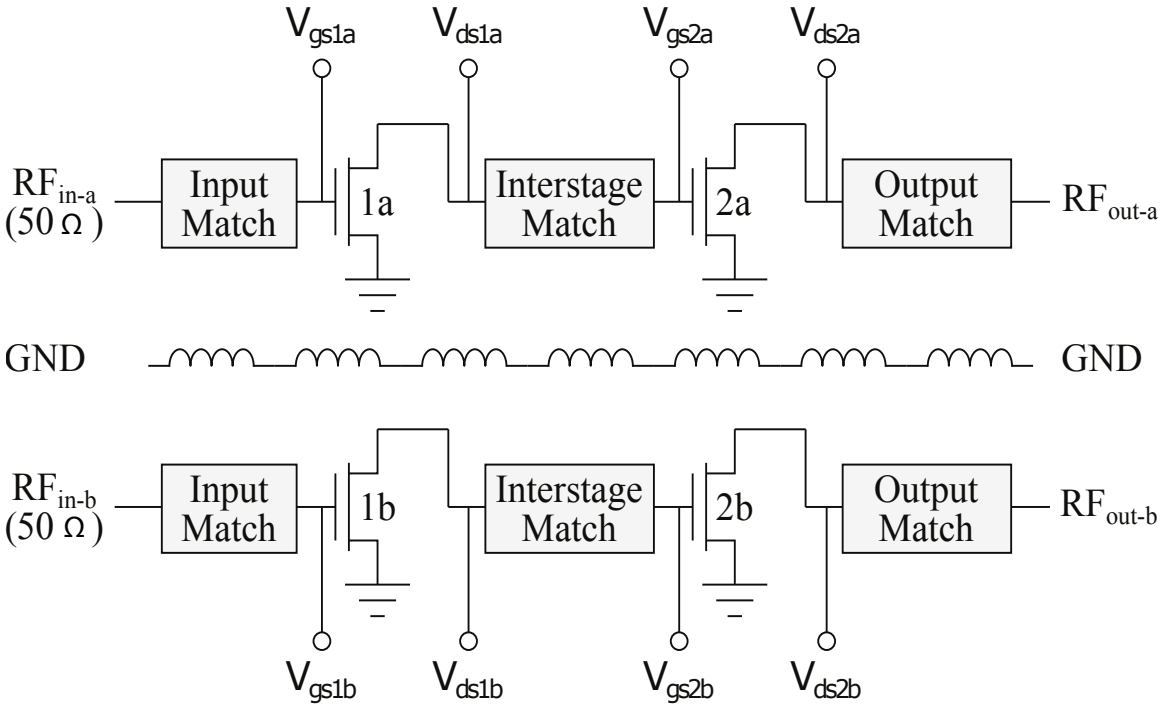

Figure 5: Integrated RF Power Transistor[7]

networks are on the same die. Integrated transistors are typically used for lower power (up to 50 Watts saturated power), higher gain and as driver stages for macro cell base stations.

The main components of a typical IC Power Transistor are :

- Input Match : This is a passive network which transforms the impedance at the gate of the first stage FET (1a,1b) to 50 Ohms (typically).
- Interstage Match : This passive network is used to perform impedance matching between the output of the first stage (1a,1b) and the input to the second stage (2a,2b). The output to the first stage must be matched to provide sufficient drive level power to the second stage while maintaining high gain and efficiency.The input to the second stage is typically a conjugate match to the FET input impedance to achieve maximum gain. It is also designed to ensure stability to prevent out-of-band oscillations.

- Output Match : This passive network is used to obtain the best combination of output power, efficiency and linearity that may be achieved by the output device. Its design is critical as any dissipative or reflective loss in this section degrades output power and power added efficiency of the overall integrated transistor. The impedance matching could be to an intermediate value or it could be matched to 50Ohms.

Typically, very high power transistors (> 100W) are suited for discrete implementations whereas low to medium power multi-stage transistors are realized in an integrated circuit form. Discrete Transistor packages are usually of the ceramic type and are higher in cost than the low cost plastic packaging that is used for lower power RF integrated circuits. ABI Research has found that the majority of low cost packaging will continue to be plastic (for power levels approimately below 100W). Plastic had about 46 % of the market revenue and 60% of the unit shipments in 2014 [8].

In mMIMO (Massive Multi-Input Multi-Output) systems, a combination of 32, 64 or128 PA transmit chains are used in the place of a single high power PA. This system has shown to provide a 3x improvement in data throughput but so far has shown to have a higher implementation cost due to the multiple RF signal paths. In the case of multiple low power PAs used in this type of system, this lends itself to an multi-stage integrated circuit implementation in plastic packaging for space as well as cost reasons.

2.4 Impedance Matching Networks

For high power transistors, the terminal impedances can be very low due to input and output device capacitances as well as due to the number of individual FET fingers connected in parallel. Hence it is necessary to provide some level of impedance transformation before the power transistor can be matched at the printed circuit board (PCB).

Two types of Matching networks are used for pre-matching power transistors :

- Parallel Inductance Matching : This type of matching network consists of a inductance connected in a shunt configuration across the device gate or drain terminal as shown in Figure 6. It serves to resonate the device capacitance at the frequency of operation. It provides a high-pass filter response to the transistor forward transmission gain. The insertion loss of this type of match is dependent on the realization of the shunt inductor (bondwires or printed spirals). Bondwires have lower losses since they are realized using Cu, Au, Al or their alloys. Printed spirals have higher losses since they are typically realized with thin metallization layers and on very thin die on lossy substrates. The blocking capacitor functions as an RF Short and thus is a high value capacitor. Technologies such as MOS-Caps or Ceramic Capacitors typically show lower quality factors above 100pF. However, high performance capacitors fabricated on high resistivity substrates can be made to be low-loss (for example, a Transmission Line Metal-Insulator-Metal Capacitor from ATC/AVX). Thus this topology has the ability to provide a low loss impedance transformation for the output of a power transistor.

- T-Section Matching : This type of matching network consists of a Series-Inductor, Shunt-Capacitor, Series-Inductor connection across the device gate or drain terminal as shown in Figure 7. It serves to provide a stepped impedance transformation and provides a low-pass filter response to the transistor forward transmission gain. The inductors are typically realized using bondwires and the capacitor could be a MOS-Capacitor or a MIM (Metal-Insulator-Metal) Capacitor realized on a high resistivity & low loss tangent substrate. The Capacitor values can range from 10pF to 100pF depending on the transistor periphery. This topology results in a higher quality factor filter response and narrower

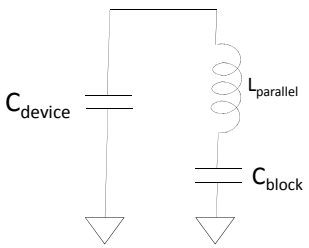

Figure 6: Parallel Inductance Matching

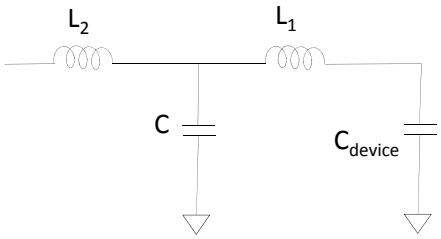

Figure 7: T-Section Matching

bandwidth than the previous matching technique. More sections can be added (L-C Ladder) for realizing a higher order filter response for improved matching bandwidth, but can increase the total loss due to the additional inductors and capacitors.

2.5 Class AB Power Amplifiers

Table 2 shows the classical modes of operation for power amplifiers[9] . The bias point and quiescent current are normalized to 1 in this table.

Under idealized conditions, the drain current can be modeled as :

$$i_d(\theta) = \frac{I_{max}}{1 - cos(\alpha/2)}[cos(\theta) - cos(\alpha/2)] \tag{3}$$

where I_{max} is the peak current that can be obtained out of a device and α is the entire conduction angle for the current. This idealized current model is only roughly approximated in physical devices, but serves to illustrate trade-offs between modes of PA operation.

Table 2: Classical Modes of Operation [9]

Mode	Bias point(Vq)	Quiescent current	Conduction angle
A	0.5	0.5	2π
AB	0 - 0.5	0 - 0.5	π-2π
B	0	0	π
C	<0	0	0-π

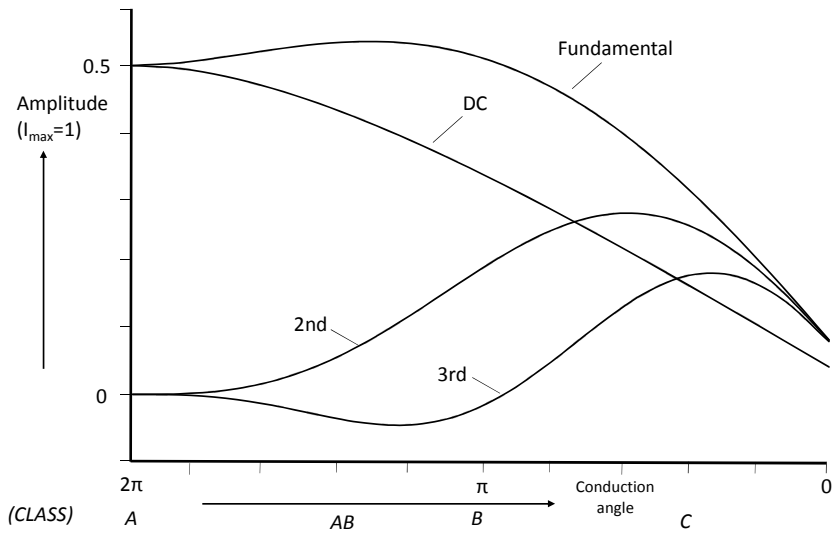

Figure 8: Fourier analysis of Drain Current Waveform [9]

If we conduct a Fourier analysis on the current waveform , we obtain :

$$I_{dc} = \frac{1}{2\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1 - \cos(\alpha/2)} [cos(\theta) - cos(\alpha/2)] d\theta \tag{4}$$

$$I_n = \frac{1}{\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1 - \cos(\alpha/2)} [cos(\theta) - cos(\alpha/2)] cos(n\theta) d\theta \tag{5}$$

where I_{dc} is the DC component of the current waveform and I_n corresponds to the magnitude of the n^{th} harmonic [9].

The above equations are plotted as a function of the conduction angle in Figure 8. [9]. It can be seen that the DC component decreases as the conduction angle is reduced. Also, the fundamental component for the Class B condition is the same as the fundamental component for the Class A condition. Hence it can be seen moving from Class A to Class B, we can improve the efficiency from 50% to 78.5%. Moving towards Class C operation, the DC as well as the fundamental component of the current continues to drop which results in higher efficiency but lower Power Utilization

Factor (PUF). PUF represents the effect of the gain reduction of a particular mode of operation compared to a class-A amplifier. It is the ratio of the RF Power delivered by a device in a particular mode under consideration to the power it would deliver as a simple class A amplifier [9].

For Class AB operation, the conduction angle is a function of drive level. Therefore, a class-AB amplifier will induce some amount of envelope distortion in an amplitude-modulated (AM) signal. However, at least for this idealized current model, class-AB mode produces a higher amplitude than class-A mode, possible resulting in a PUF greater than unity over a limited range of conduction angle. If we consider a strongly limiting transconductive device (which has a perfectly linear region between the cutoff and saturation points, but sharply limits beyond this range),the Class AB mode shows a substantial softening of the power transfer characteristic above the level of drive where cutoff starts to occur. However, if we also consider weaker nonlinearities in the transconductance properties that appear in physical devices, a Class-AB bias condition can be found that has a more linear characteristic over a wider dynamic range than the Class A mode due to the cancellation of distortion products produced by the separate nonlinear characteristics. This linearity 'sweet-spot' is dependent on device technology, operating mode and RF load impedance, but is regularly achieved in practical PA designs [9].

2.6 Doherty Power Amplifiers

RF Power Amplifiers designed for Base Station applications are required to support multiple modulation schemes such as Multi-Carrier GSM, Wide-band CDMA, CDMA and Long Term Evolution (LTE). Use of complex modulation schemes such as LTE and orthogonal frequency division multiplexing (OFDM) result in signals with a high peak to average power ratio. This motivates the use of Doherty Power Amplifiers that provide high efficiency over a wider dynamic range.

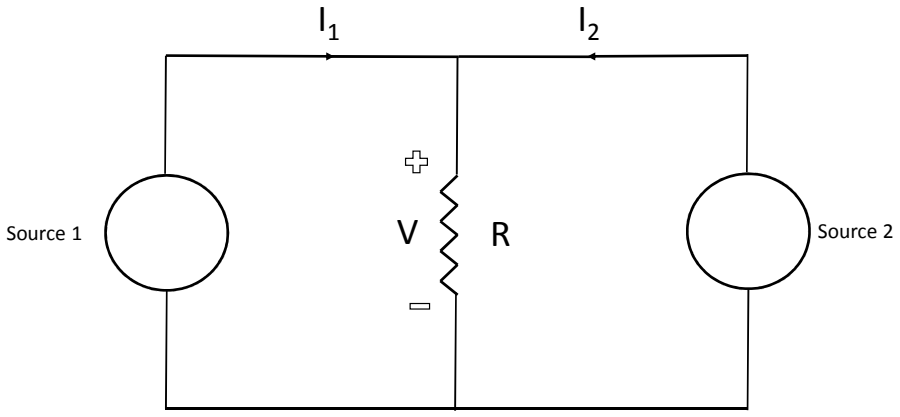

Figure 9: Active Loadpull Technique

The Doherty Architecture was introduced by W.H. Doherty in 1936. [10]. The principle of operation of the Doherty amplifier can be explained using the active load-pull model.

From Figure 9, the voltage across resistor R can be written as :

$$V = (I_1 + I_2)R \tag{6}$$

The resistance (load) seen at the terminals of Source 1 (R_1)is :

$$R_1 = R\frac{I_1 + I_2}{I_1} \tag{7}$$

The resistance (load) seen at the terminals of Source 2 (R_2)is :

$$R_2 = R\frac{I_1 + I_2}{I_2} \tag{8}$$

It can be seen from the equations that the load seen at the terminals of Source 1 can be modulated by controlling the current out of Source 2 and vice versa.

This analysis can be represented in a generalized form as :

$$Z_1 = R\frac{I_1 + I_2}{I_1} \tag{9}$$

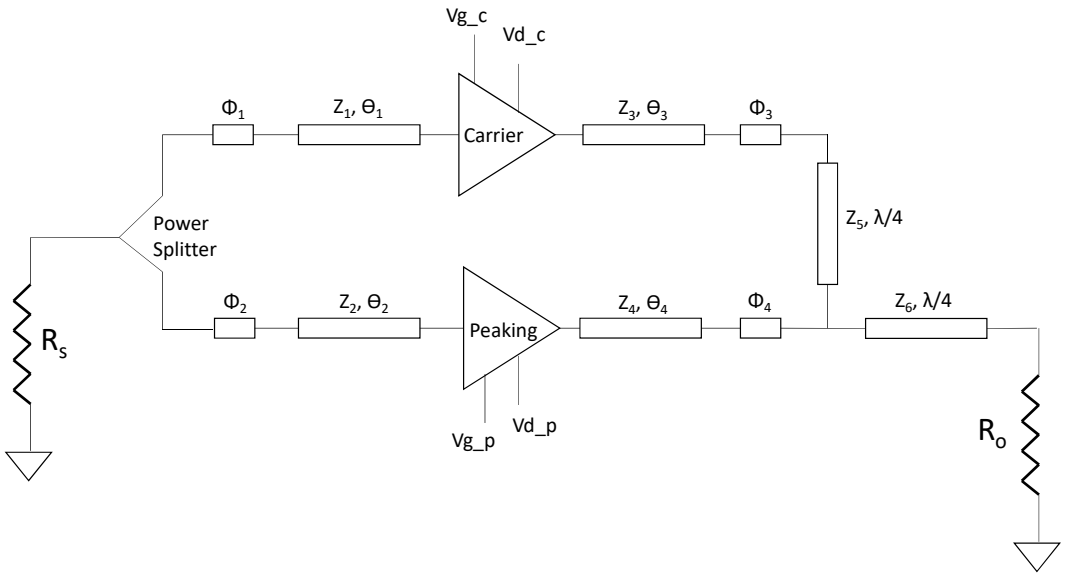

Figure 10: Conventional Doherty Architecture

$$Z_2 = R\frac{I_1 + I_2}{I_2} \tag{10}$$

where Z_1 and Z_2 are impedances and I_1 and I_2 are complex phasor quantities. Figure 10 shows the architecture of a conventional Doherty topology.

- R_o represents the system impedance which is typically 50 Ohms.
- The power splitter is designed to provide the required power coupling between the paths. For a symmetric Doherty, this is an equal power (3dB) split.
- Transmission Lines Z_1, Z_2, Z_3 and Z_4 are are designed to transform the power transistor impedances to the system impedance or an intermediate value to best optimize power output and efficiency.
- The phase delays of the transmission lines ϕ_1, ϕ_2, ϕ_3, ϕ_4 function as phase alignment components to best ensure that the power out of the Carrier and Peaking paths combine in phase at the combining node.

- Transmission Line Z_5 functions as a quarter-wave transformer to transform the impedance of the Peaking amp (as modified by Z_4 and ϕ_4) to effectively modulate the load impedance presented to the carrier path.

- Transmission Line Z_6 functions as an impedance transformer which enables high efficiency operation by presenting a higher load impedance to the Carrier Path during low power conditions thus achieving Doherty operation.

- Bias connections Vg_c, Vd_c, Vg_p and Vd_p provide biasing voltages to the Carrier and Peaking Transistors. The carrier amplifier is typically biased in class-AB mode because it is providing the output power for all amplitudes below the peaking level. The Peaking amplifier is biased in class-C so that it only contributes to the output power above the peaking level.

A Doherty PA is bandwidth limited due to several factors [11] :

- Limited bandwidth of matching networks for the individual PAs.

- Optimal load modulation that requires different impedances at different power levels.

- Impedance inverters which are typically realized by means of a quarter-wave transmission lines which are intrinsically narrow-band.

- Offset lines are well-defined for a single frequency operation.

- Adoption of harmonic terminations which are typically realized using resonant narrow-band circuits.

- A high off-state impedance is required by the peaking amplifier when the input level is below the threshold. Since the peaking output is a frequency dependent impedance, its loading effect on the combiner will vary across frequency. This

will cause unwanted variation in the impedance seen by the carrier amplifier across frequency.

The above band-limiting factors can lead to significant short-term memory effects in the behavior of the Doherty Power Amplifier which can make DPD correction more complex as discussed in the next section.

2.7 Digital Pre-Distortion

A Digital Pre-Distortion (DPD) System is typically a closed looped system that works in conjunction with a Power Amplifier to create a minimally distorted output spectrum. A Predistortion Linearizer essentially generates a non-linear transfer characteristic which is an inverse of the PA's transfer response in both magnitude and phase and thus causes a cancellation of the distortion produced by the power amplifier [12].

For narrow bandwidth signals, nonlinearity in the PA can be modeled using a simple polynomial structure with complex coefficients to treat amplitude and phase distortion.For such narrowband operation, polynomial models may be estimated by comparing the PA output waveform to the original input waveform, and minimizing the error in lease-square fashion. A generic Taylor series model for the PA is described in [13], where the authors shows that the coefficients of the model can be acquired directly from the intercept points of the PA. However, this only applies at high back-off levels, implying inefficient PA operation.

Once a PA polynomial model is generated, an inverse predistortion function can also be expressed as a polynomial (i.e. the polynomial pre-inverse), as shown in figure 11. Nonlinear element (Block A) is preceded by another nonlinear component (Block B) such that the cascade of the two elements behaves as a linear system H.

Figure 12 shows a block diagram of an adaptive DPD System. [13]. It consists of a Digital Block that serves to generate the input signal as well as its distorted components in baseband. A functionality known as Crest Factor Reduction is also

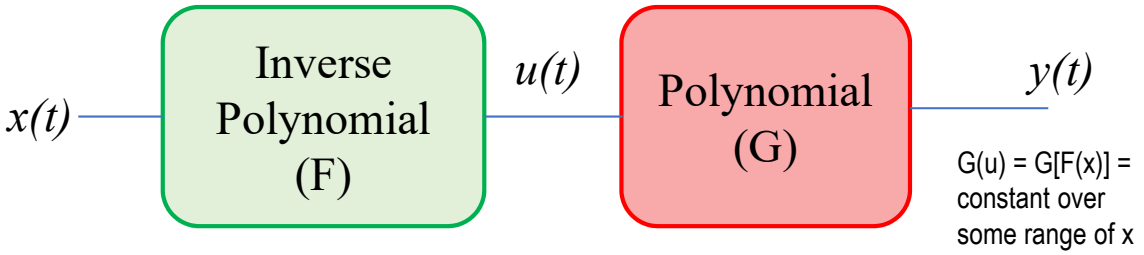

Figure 11: Mathematical Modeling of the pre-distortion system

implemented here and it serves to reduce the peak to average ratio of the input signals. As discussed in the next section, more complex DPD systems that employ Volterra-based models are based on the same architecture as shown in Fig.12.

2.8 Volterra Series and Memory Effects

Consider a polynomial model that describes a nonlinear system [14][15][16]:

$$y(t) = a_0 + \sum_{n=1}^{N} a_n u^n(t) \tag{11}$$

Expanding into a Taylor series around some operating point u_0 :

$$y(u(t)) = y(u)|_{u=u_0} + \frac{1}{2!}\frac{dy}{du}|_{u=u_0}(u-u_0) + \frac{1}{3!}\frac{d^2y}{du^2}|_{u=u_0}(u-u_0)^2 + ... \tag{12}$$

$$y(u(t)) = a_0 + a_1 u + a_2 u^2 + ... \tag{13}$$

If we allow y(t) to be a function of u(t) as well as its value at some past times,

$$y(t) = f(u, u_1, ..., u_n) \tag{14}$$

where the input signals delayed by τ_i are given as

$$u = u(t), u_1 = u(t-\tau_1), u_2 = u(t-\tau_2), ... \tag{15}$$

Expanding this form into a Taylor series :

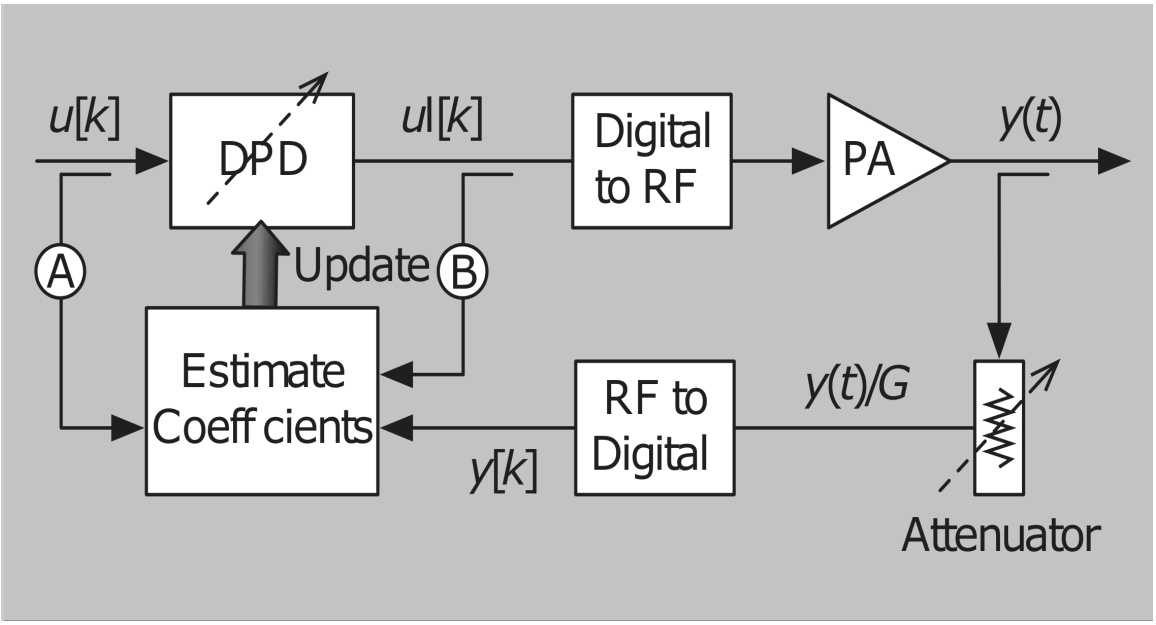

Figure 12: Digital Pre-Distortion System [13]

$$\begin{aligned} y(u(t)) = y(u)|_{u=u_0} + \frac{1}{2!}\frac{dy}{du}|_{u=u_0}(u-u_0) + \frac{1}{2!}\frac{dy}{du_1}|_{u=u_0}(u-u_0) + ... \\ \frac{1}{3!}\frac{d^2y}{du^2}|_{u=u_0}(u-u_0)^2 + \frac{1}{3!}\frac{d^2y}{du_1^2}|_{u=u_0}(u_1-u_0)^2 + ... \\ \frac{1}{3!}\frac{d^2y}{dudu_1}|_{u=u_0}(u-u_0)(u_1-u_0) + ... \end{aligned} \tag{16}$$

Because the Eq. (16) may be expressed in matrix form, the terms in $(u_1 - u_0)$ are called the diagonal memory terms and the terms in $(u - u_0)(u_1 - u_0)$ are referred to as the Volterra Cross Terms. Thus, the Volterra Series can be considered to be akin to a Taylor Series with memory.

Electrical systems can be classified into one of four types as shown in Table 3. [14]

An energy storing element adds memory to the system by the integration of current or voltage. For example, the instantaneous voltage across a capacitor is a function of all prior current values as shown in the equation below.

$$v_c(t) = \frac{1}{C}\int_{-\infty}^{t} i(t')dt' \tag{17}$$

Table 3: Classification of Electrical Systems[14]

	Memoryless	With Memory
Linear	Linear Resistance	Linear Capacitance
Non-Linear	Non-Linear Resistance	Non-Linear Capacitance or Non-Linear Resistance and Linear Capacitance

In the time domain, memory effects cause the time response of the circuit to be convolved by the impulse response of the system. In the frequency domain, memory effects result in a frequency dependent gain and phase shift of the signal.

Memory effects can also be classified as bandwidth-dependent effects. These effects can be studied by applying a two-tone input signal with varying tone spacing. If we model a system by a third degree polynomial as :

$$y = a_1.x + a_2.x^2 + a_3.x^3 \tag{18}$$

and use a two-tone signal as the input excitation, we see that the generated third order intermodulation distortion components (IM3) are not functions of tone spacing and their magnitude increases to the third power of the input amplitude.

However a comparison between the polynomially modeled and actual phases of IM3L as a function of tone spacing shows large differences between the two. The real amplitude and phase of the IM3 component may deviate at low and high modulation frequencies indicating the existence of signal bandwidth dependent nonlinear effects with memory (Figure 13).

These memory effects can be resulting from Electro-Thermal effects (below 100kHz modulation frequencies) within the active device and Electrical effects (several MHz modulation frequency) that result from the interaction of the active device with the

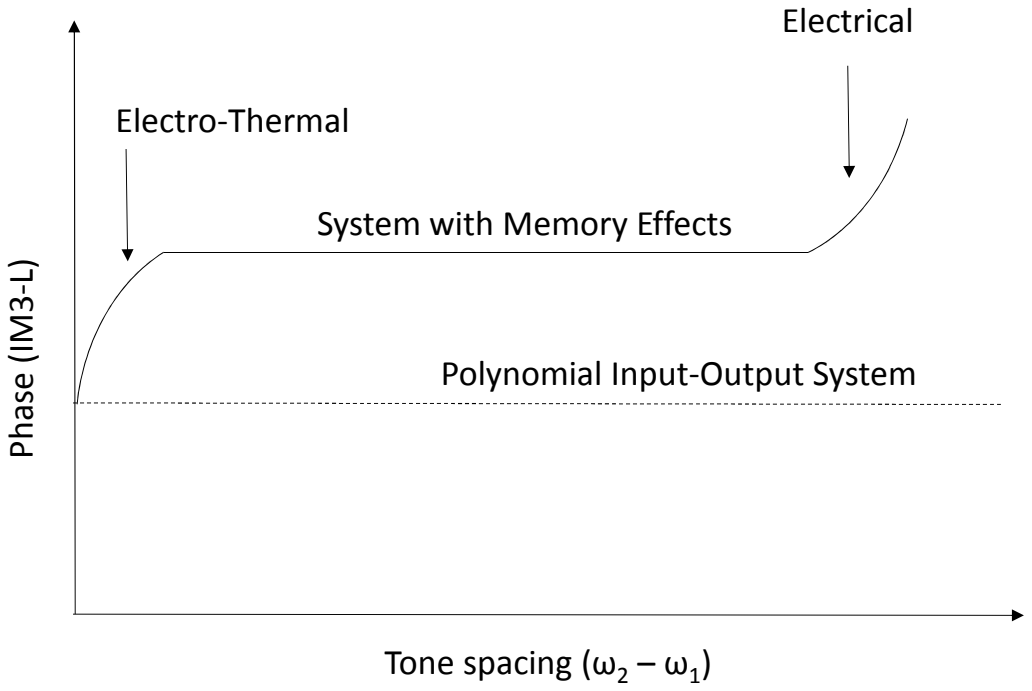

Figure 13: Phase of the IM3 component of a system with (solid line) and without (dashed line) memory effects. [17]

reactive components that are connected to it. Trap-related effects also contribute to memory effects in certain deice materials such as GaAs and GaN.

To model these memory effects, we can represent the transistor amplifier as a cascade of two nonlinearities as shown in Figure 14.

For Field Effect Transistors, block H represents the gate voltage as a function of the input signal, while block F represents the drain voltage as a function of the gate voltage. H_1, H_2 and H_3 represent different order blocks which correspond to the coefficients a_1, a_2 and a_3 respectively in the polynomial input-output model. IM3 components are generated by the cascaded third and second degree nonlinearities. These are affected not only by the fundamental voltage waveforms, but also by the voltage waveforms of the different nodes at the envelope and second harmonic frequencies.

Since the nonlinearities of the circuit components can be regarded as current

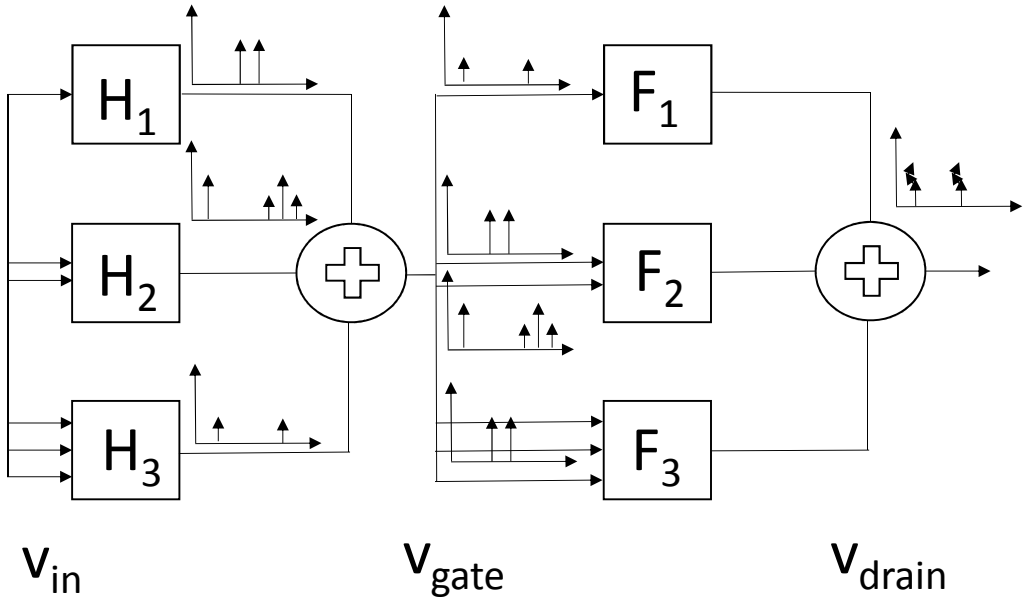

Figure 14: Representation of the Cascade Connection with Volterra Operators of the order one to three. [18]

sources, their voltage waveforms can be affected by node impedances. Thus electrical memory effects are caused by frequency-dependent envelope, fundamental or second harmonic impedances.

2.9 Video-Bandwidth

In a general form, Video-Bandwidth can be defined as the modulation bandwidth over which the response of the PA is relatively free of bandwidth related memory effects. If we subject an RF Power Amplifier to a two tone input signal with constant input power and monitor the output spectrum as we sweep the tone spacing, we obtain a response similar to the one shown in Figure 15. Here we define three different response behaviors :

- Condition 1 : This condition points to an amplitude asymmetry between the IMD3 components as we vary the tone spacing. A high level of asymmetry is

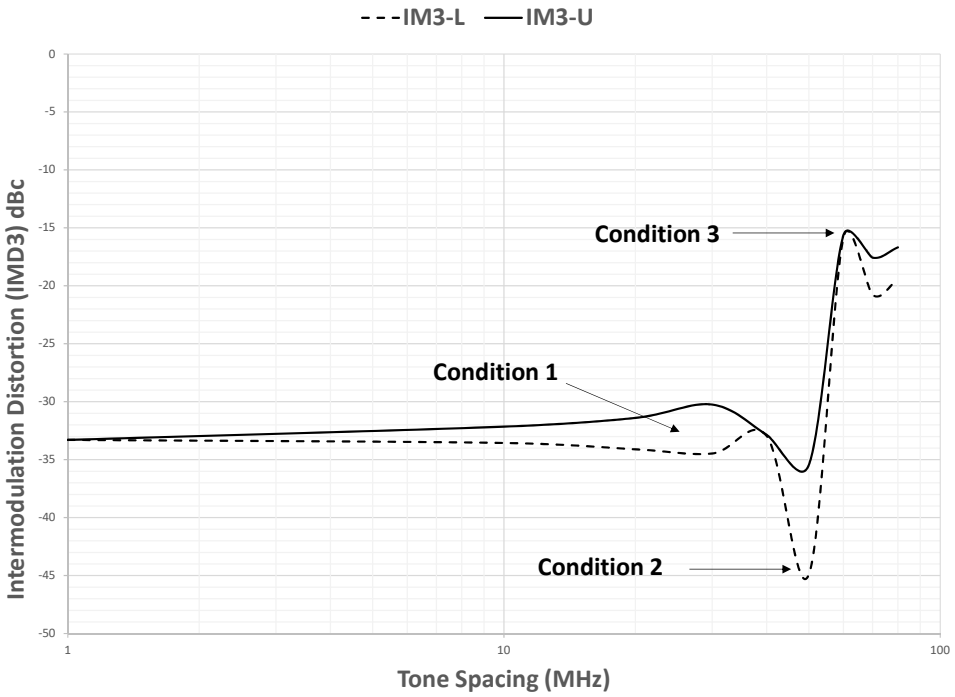

Figure 15: Two Tone Test showing IMD3 vs. Tone Spacing

an indication of increased bandwidth related memory effects.

- Condition 2 : This condition points to the onset of resonance and can be construed as the absolute maximum signal bandwidth that can be amplified by this PA without incurring severe distortion.

- Condition 3: This condition represents the actual resonance and it points to a envelope impedance resonance in the bias circuit of the PA.

  For the purposes of this research, we adopt Condition 2 as the criterion to assess the Video-Bandwidth Capability of an RF Power Transistor.

CHAPTER III

PROBLEM STATEMENT

Large Periphery devices used in High Power RF Transistors are inherently bandwidth limited due to the large capacitances present at their gate and drain terminals. As was discussed in Section 2.8, one of the key contributors to electrical memory effects is the variation of the envelope impedance with frequency. There are two components to the envelope impedance as presented to the transistor : Gate Baseband Impedance and Drain Baseband Impedance, referring to the envelope impedance presented to the Gate and Drain of the Power Transistor respectively.

3.1 Gate Baseband Impedance

A simplified low frequency equivalent circuit for the gate of a pre-matched power transistor is shown in Figure 16.

R_{gs} and C_{gs} represent Gate-Source resistance and capacitance. C_{gs} is usually a function of applied voltage. L_1, C_1 and L_2 are impedance pre-match components that transform the die level impedances to some higher intermediate value for ease of matching on a PCB. TL_1 represents a quarter wave micro-strip line that is used to provide the gate bias to the Package Lead of the transistor. C_2 represents a bias decoupling capacitor whose value can be between 0.1μF to 47μF. Usually, two or more high value capacitors are used here, sometimes in a decade decoupling configuration. A low value capacitor is used to provide a short at the fundamental frequency followed by several high value decoupling capacitors. Any PCB trace between the RF Short and decoupling capacitors will add some inductance. The impedance presented to the intrinsic gate is shown in Figure 17.

Estimated values for L1 & L2 are in the range of 100pH to 500pH in a high

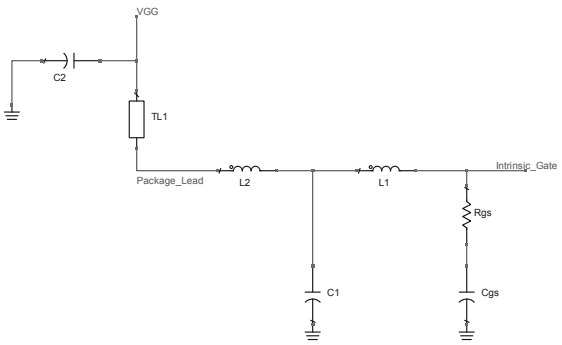

Figure 16: Low Frequency Equivalent Circuit for the Gate of a pre-matched LDMOSFET

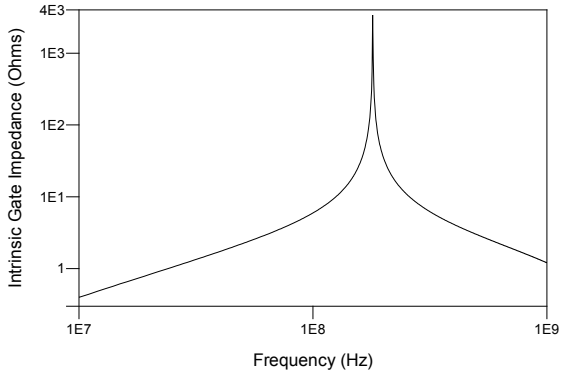

Figure 17: Impedance Presented to the Intrinsic Gate of the FET as a function of Frequency

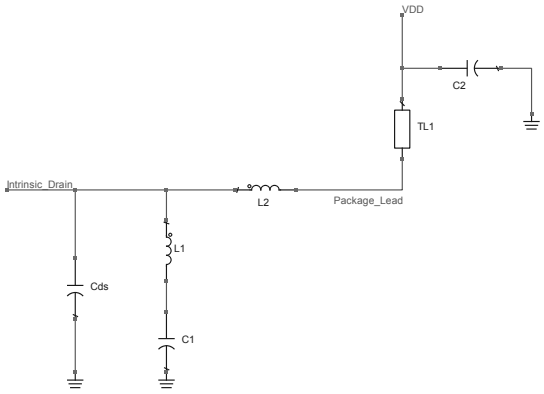

Figure 18: Low Frequency Equivalent Circuit for the Drain of a pre-matched LDMOSFET

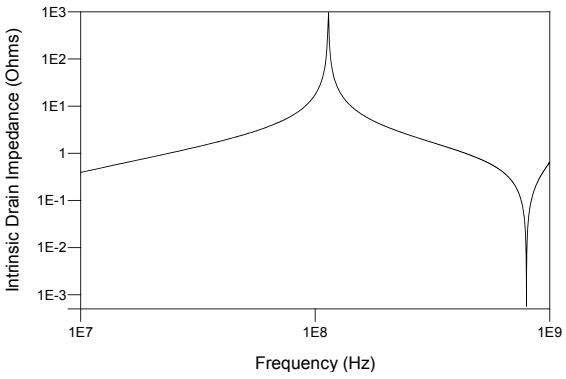

Figure 19: Impedance Presented to the Intrinsic Drain of the FET as a function of Frequency

power transistor. It can be seen that in the baseband region, the combination of the pre-match and PCB biasing circuit is presenting a sharp resonance at 180MHz. The component values used are typical of a 100W power transistor.

3.2 Drain Baseband Impedance

A simplified low frequency equivalent circuit for the drain of a pre-matched power transistor is shown in Figure 18.

C_{ds} represent Drain-Source Capacitance of the LDMOSFET. C_{ds} is usually a function of applied voltage. L_1, C_1 and L_2 are impedance pre-match components that transform the die level impedances to some higher intermediate value for ease of matching on a Printed Circuit Board. TL_1 represents a quarter wave microstrip line that is used to provide the drain bias to the Package Lead of the transistor. C_2 represents a bias decoupling capacitor whose value can be between 0.1μF to 47μF. The impedance presented to the intrinsic drain is shown in Figure 19.

It can be seen that in the baseband region, the combination of the pre-match and PCB biasing circuit is presenting a sharp resonance at 114MHz. The component values used are typical of a 100W power transistor.

Thus the envelope impedances presented to the intrinsic gate and drain of the FET not only vary as a function of frequency, but also exhibit sharp resonances. Hence, to improve the Video-Bandwidth of a power transistor, it is important to modify the resonance behavior of the envelope impedance to be low in magnitude and free of resonances in the envelope frequency region.

An observation of the behavior of the baseband resonances shows that these can be modeled as the impedance response of a parallel resonant circuit. The resonant frequency of such a circuit f_{res} is given by :

$$f_{res} = \frac{1}{2\pi\sqrt{L_{res}C_{res}}} \tag{19}$$

where L_{res} and C_{res} are the equivalent shunt inductance and shunt capacitance respectively.

In the case of the Gate Baseband Impedance, L1,L2,TL1(equivalent low frequency inductance) and C_2 (usually a high value capacitor which has a very low self resonant frequency and can be assumed to behave as an inductor at the frequencies of interest) can be thought of as comprising L_{res}. C_{gs} & C_1 can be thought of as comprising C_{res}.

Similarly on the case of the Drain Baseband Impedance, L1,L2,TL1 and C_2 can

be thought of as comprising L_{res}. C_{ds} & C_1 can be thought of as comprising C_{res}.

Thus, a reduction in either C_{res} or L_{res} can result in a higher resonant frequency and a lower baseband impedance in the envelope frequency region. However, all components in the described equivalent circuit have a specific function and thus varying their values may perturb other parameters of the transistor.

For example, C_{gs} and C_{ds} are fixed by the technology and periphery of the power transistor. Inductors L_1,L_2 and capacitor C_1 serve as impedance matching components and their values are based on the fundamental frequency of operation. Transmission line TL_1 can be modified for lower inductance by varying its width, but its impact on the resonance frequency would be a few tens of MHz. Capacitor C_2 is typically fixed in its self inductance and is usually small compared to other inductive elements.

Thus there is a need for a technique to increase the resonant frequency of the Gate and Drain Baseband Circuits by a significant amount, above those achievable by small changes in existing matching and PCB components.

The non-idealities in passive structures can be a significant contributor to distortion. As an example, capacitors used on bias lines as decoupling elements are made up of materials that vary in their response to temperature and voltage changes. The two main type of capacitors are:

- High Dielectric Type Capacitors, such as those with X5R & X7R characteristics. The material used in these types of capacitors is ferroelectric barium titanate ($BaTiO_3$). The dielectric constant can vary from 1000 to 20,000 at room temperature, which enables a larger capacitance density. However, the dielectric constant is a function of temperature and voltage. These capacitors are suitable for bypass and decoupling applications.

- Temperature Compensating Type Capacitors, such as those with C0G characteristics. The material used in these types of capacitors is Paraelectric Titanium Oxide (TiO_2) or Calcium Zirconate ($CaZrO_3$). The relative dielectric constant is between 20 - 300. The relative dielectric constant for this material changes almost linearly with temperature. Under extreme conditions (high temperature, high voltage, high frequency), the loss tangent remains low and the dielectric is stable. Capacitors using this dielectric find use in high frequency circuits as matching elements.

CHAPTER IV

THE PROPOSED SOLUTIONS

4.1 Common Source Amplifier Volterra Kernels [19]

The Volterra Series is a general nonlinear model with memory and has been used to model PAs with mild nonlinearities. The drain current of a MOSFET operating in a common source configuration can be given as [20] :

$$I_d = \beta(V_{gs} - V_T)^{\gamma} tanh(\alpha V_{ds})(1 + \lambda V_{ds}) \tag{20}$$

where α controls the knee region sharpness; β is related to the maximum drain current and γ varies based on the model.

Assuming a weakly nonlinear system for the purposes of this analysis, we can set γ=3 (to account for third order nonlinearities) and ignore α and λ. Representing the drain current as a function of the gate to source voltage :

$$I_{out} = (-V_T^3\beta) + (3V_T^2\beta)v_{in} + (-3V_T\beta)v_{in}^2 + (\beta)v_{in}^3 \tag{21}$$

where I_{out} is the drain current and v_{in} is the gate-source voltage.

Setting the load impedance presented to the FET in the form of a parallel LC circuit, where C includes the device drain-source and pre-matching network capacitances and L covers bias line and pre-matching inductances. Referring to the analysis for a nonlinear amplifier in [21], we can show that the first three Volterra kernels of this system can be written as :

$$H_1(j\omega) = (-3V_T^2\beta)\frac{\omega L}{1 - \omega^2 LC} \tag{22}$$

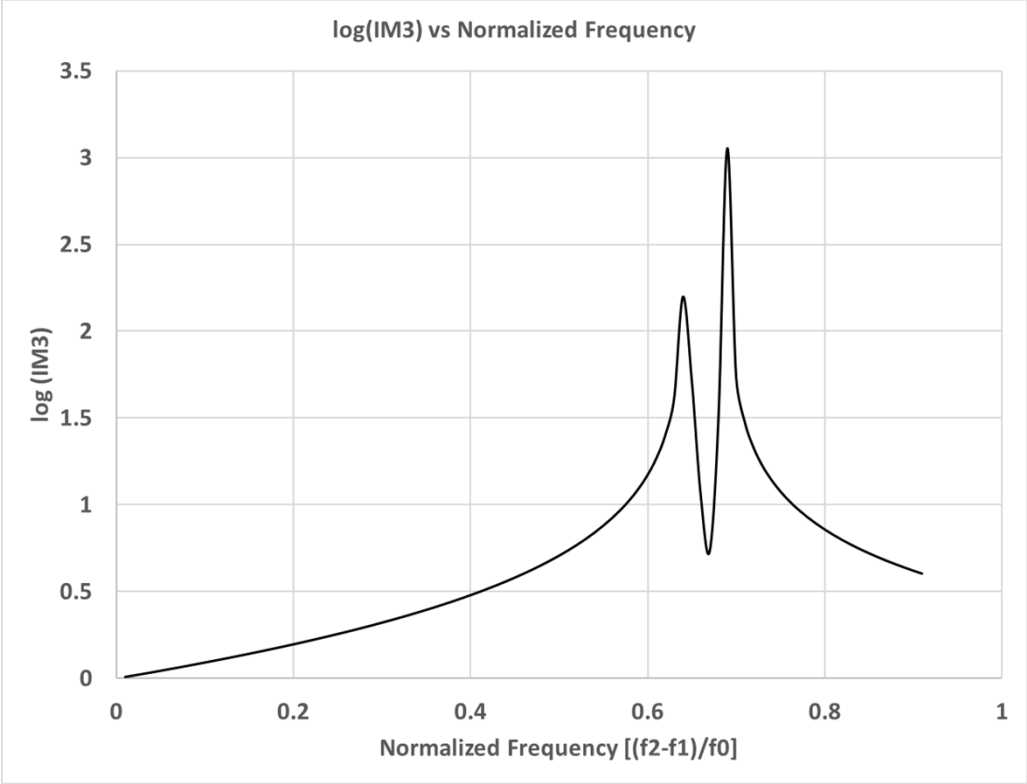

Figure 20: IM3 as a function of Normalized Delta Frequency [19]

$$H_2(j\omega_1, j\omega_2) = (3V_T\beta)\frac{(\omega_1+\omega_2)L}{1-(\omega_1+\omega_2)^2LC} \tag{23}$$

$$H_3(j\omega_1, j\omega_2, j\omega_3) = (-\beta)\frac{(\omega_1+\omega_2+\omega_3)L}{1-(\omega_1+\omega_2+\omega_3)^2LC} \tag{24}$$

The third order intermodulation distortion product is is then written as [19]

$$IM3 = \left|\frac{H_3(j\omega_1, -j\omega_2, -j\omega_2)}{H_1(j\omega_1)}\right| \tag{25}$$

$$IM3 = \frac{1}{3V_T^2}\frac{1-\omega_1^2LC}{1-(\omega_1-2\omega_2)^2LC}\frac{\omega_1-2\omega_2}{\omega_1} \tag{26}$$

The dependency of the IM3 on the load network can explain the resonant behavior seen in the IMD products which was reported in [22], [23], [24], [25], [26], [27], [28],

[29]. If we consider a more complex model for the transistor load (consisting of nonlinear conductances and capacitances), it was reported by Carvalho and Pedro in [16] that the necessary condition for the existence of IMD asymmetry in small signal is the presence of a reactive part on the difference frequency terminating impedance. Figure 20 shows a plot of IM3 as a function of carrier spacing. It confirms the presence of resonant behavior in the H_3/H_1 ratio.

The Volterra series modeling has a drawback concerning the large number of coefficients that must be extracted. To capture the memory effects in PAs due to wideband signals, two special cases of the Volterra model are used : The Wiener model [30] and the Memory Polynomial Model [31]. The Memory polynomial model discussed in [32] is a simplified model based on considering only the diagonal kernel of the Volterra Series. Cross-Terms are not considered in the Memory Polynomial Model [32].

In RF Power Amplifiers, memory effects arise from three different sources : RF Frequency response (which is a short term memory effect cause by the complex gain variation across the operating band), low frequency envelope termination response due to the bias circuit interactions and electro-thermal feedback.

4.2 Common Source Amplifier Drain Network[19]

Figure 21 shows an equivalent circuit of the output of a Single Ended Common Source Power Amplifier, where C_{ds} is the drain to source capacitance of the MOSFET, L_{shunt} and C_{Block} form the pre-matching network and TL_Bias represents the bias line used to provide the drain voltage to the PA. The approximate equivalent inductance of TL_Bias can be written as

$$L_{Bias} = \frac{Z_o tan(\omega l/c)}{\omega} \tag{27}$$

where l is the length of the line in meters, $c = 3 * 10^8$ m/s and $Zo =$ characteristic

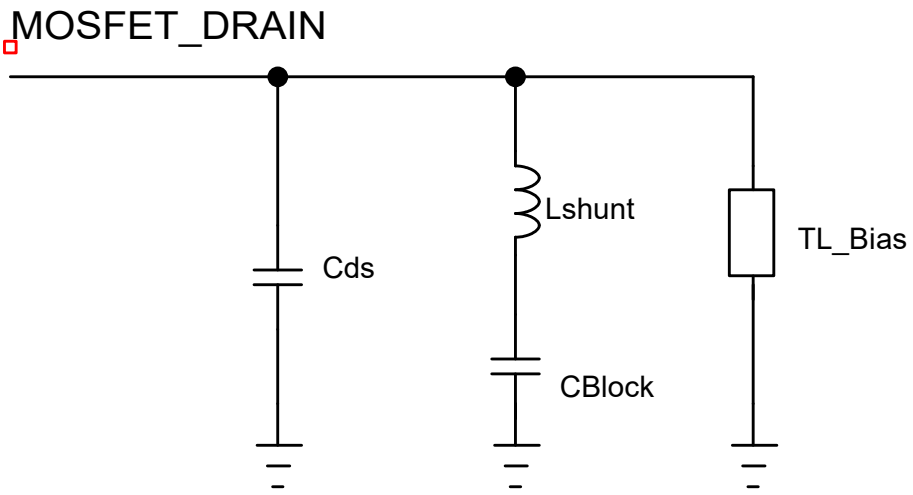

Figure 21: Equivalent Circuit representing the Output of a Single-Ended Common Source Power Amplifier[19]

impedance of the line. The impedance presented to the drain of the MOSFET for Figure 21 can be written as

$$Z_{DrainA} = j\omega \frac{L_{Bias}(1 - \omega^2 L_{shunt} C_{Block})}{1 - \omega^2 L_{shunt} C_{Block} - \omega^2 L_{Bias} \gamma} \tag{28}$$

$$\gamma = C_{ds} + C_{Block} - \omega^2 L_{shunt} C_{ds} C_{Block} \tag{29}$$

Figure 22 shows the variation of the magnitude of the impedance Z_{Drain} versus frequency. Values assumed for the parameters are for a 100mm LDMOS device designed for 2.6 GHz (as an example) with C_{ds}=24 pF, L_{shunt}=0.25nH, C_{Block}=120pF and L_{Bias}=6nH. It is observed that the this impedance is highly reactive with a resonance occuring at 170MHz. As discussed, such a resonance will degrade distortion performance, even under DPD correction, due to asymmetric IMD [16].

The bias network may be modified in such a way to suppress the unwanted resonance. However, this requires that additional bias elements be placed as close to the power transistor die as possible, which will require integration within the transistor

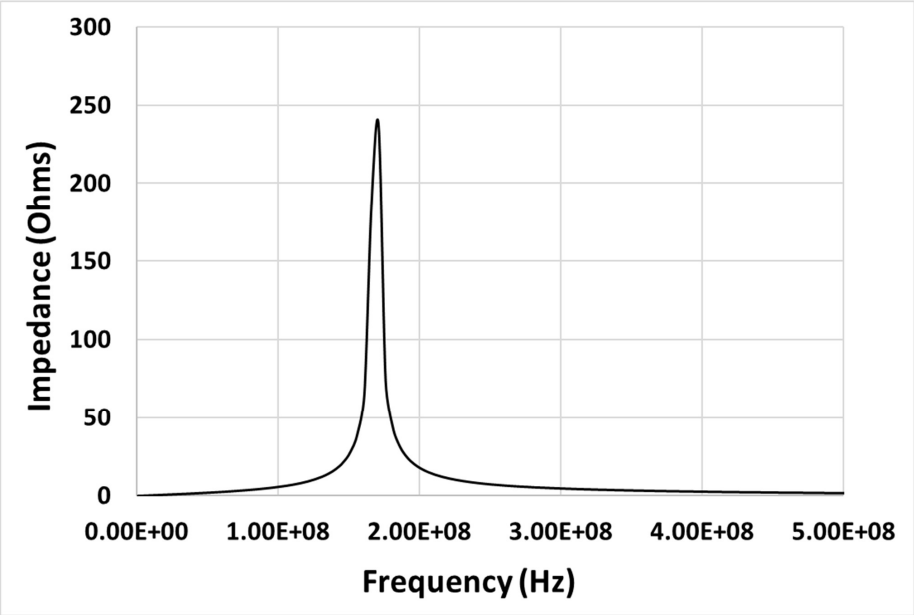

Figure 22: Magnitude of the Impedance presented to the Drain of the MOSFET by the network of Figure 21 plotted using Equation 28[19]

package. Figure 23 shows an equivalent circuit of the output of a Single Ended Common source Power Amplifier with an integrated baseband termination comprising L_{env} and C_{env} connected at the node between L_{shunt} and C_{Block}.

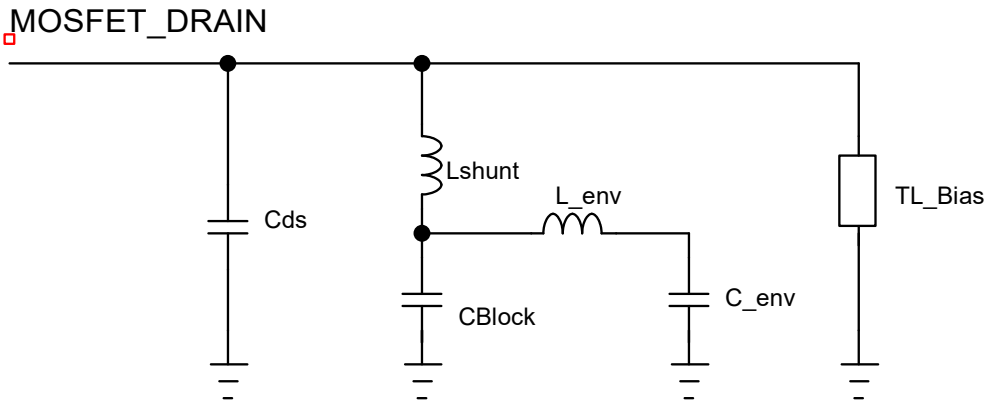

Figure 23: Equivalent Circuit representing the Output of a Single-Ended Common Source Power Amplifier with an Integrated Baseband Termination[19]

The impedance presented to the drain of the MOSFET with the integrated baseband termination can be written as

$$Z_{DrainB} = j\omega \frac{L_{Bias} - \omega^2(L_{shunt}L_{Bias}\alpha + L_{Bias}L_{env}C_{env})}{\omega^4\delta_1 - \omega^2\delta_2 + 1} \tag{30}$$

$$\delta_1 = L_{Bias}C_{ds}L_{env}C_{env} + L_{shunt}C_{ds}L_{Bias}\alpha \tag{31}$$

$$\delta_2 = L_{Bias}\alpha + L_{Bias}C_{ds} + L_{shunt}\alpha + L_{env}C_{env} \tag{32}$$

$$\alpha = C_{Block} + C_{env} - \omega^2 L_{env}C_{Block}C_{env} \tag{33}$$

Figure 24 shows the variation of the magnitude of the impedance Z_{DrainB} versus frequency. Values assumed for the integrated baseband termination are L_{env}=0.3nH and C_{env}=30nF. It is observed that the primary resonance has been shifted up to 780 MHz. Being close to the carrier frequency, this high frequency resonance will allow significant RF power to enter the bias network, degrading efficiency. However a secondary resonance is now introduced at 11 MHz. This secondary resonance will also degrade distortion performance for the same reasons previously discussed. Both primary and secondary resonances should be suppressed for proper PA operation.

Figure 25 shows an equivalent circuit for the output of a Single Ended Common Source Power Amplifier with an integrated baseband termination that includes a damping resistor R_{env}. Symbols Cds (Drain-Source Capacitance), Lshunt and CBlock (RF pre-match), L_{env}, R_{env}, C_{env} (integrated baseband termination). R_{env} functions to alleviate the resonant behavior that may occur due to the secondary resonance. The external power supply bias line quarter wave transformer is shown as TL Bias. Figure 26 shows the variation of the magnitude of the impedance seen at the drain of the MOSFET using this network for different values of R_{env}. It is observed that the sharp resonance behavior for the primary and secondary resonances has been damped by the presence of this resistor.

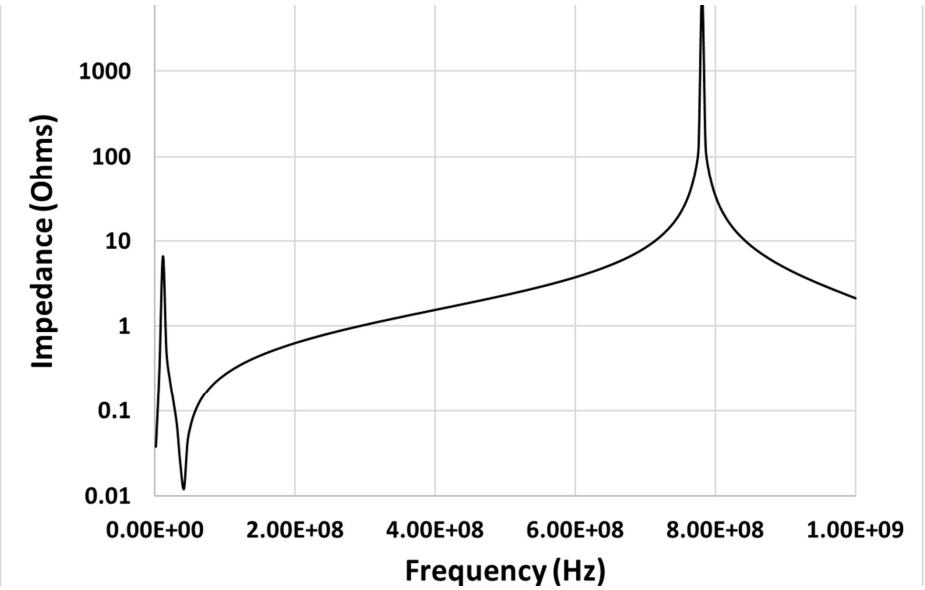

Figure 24: Magnitude of the Impedance presented to the Drain of the MOSFET by the network of Figure 23 plotted using Equation 30 [19]

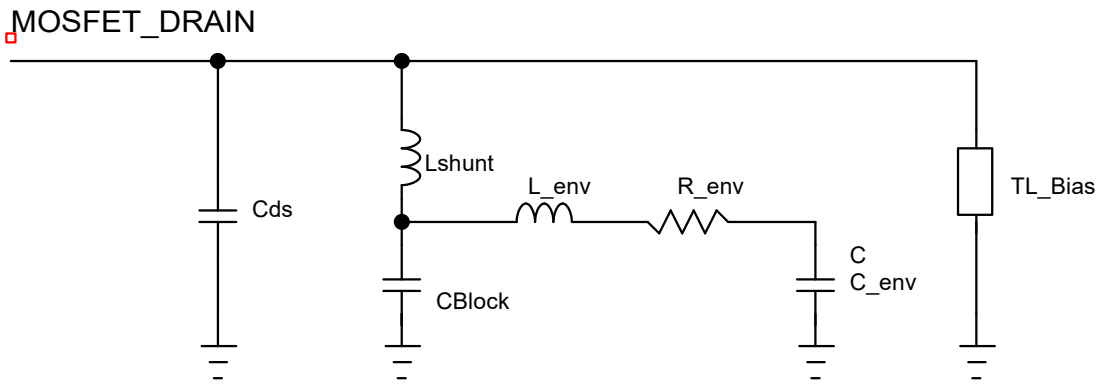

Figure 25: Equivalent Circuit representing the Output of a Single-Ended Common Source Power Amplifier with an Integrated Baseband Termination and a Damping Resistance[19]

If we include the presence of a damping resistor in the equations for H_3 and H_1, we get the following equations:

$$H_1(j\omega) = (-3V_T^2\beta)\frac{R + j\omega L}{1 - \omega^2 LC} \tag{34}$$

$$H_3(j\omega_1, j\omega_2, j\omega_3) = (-\beta)\frac{R + j(\omega_1 + \omega_2 + \omega_3)L}{1 - (\omega_1 + \omega_2 + \omega_3)^2 LC} \tag{35}$$

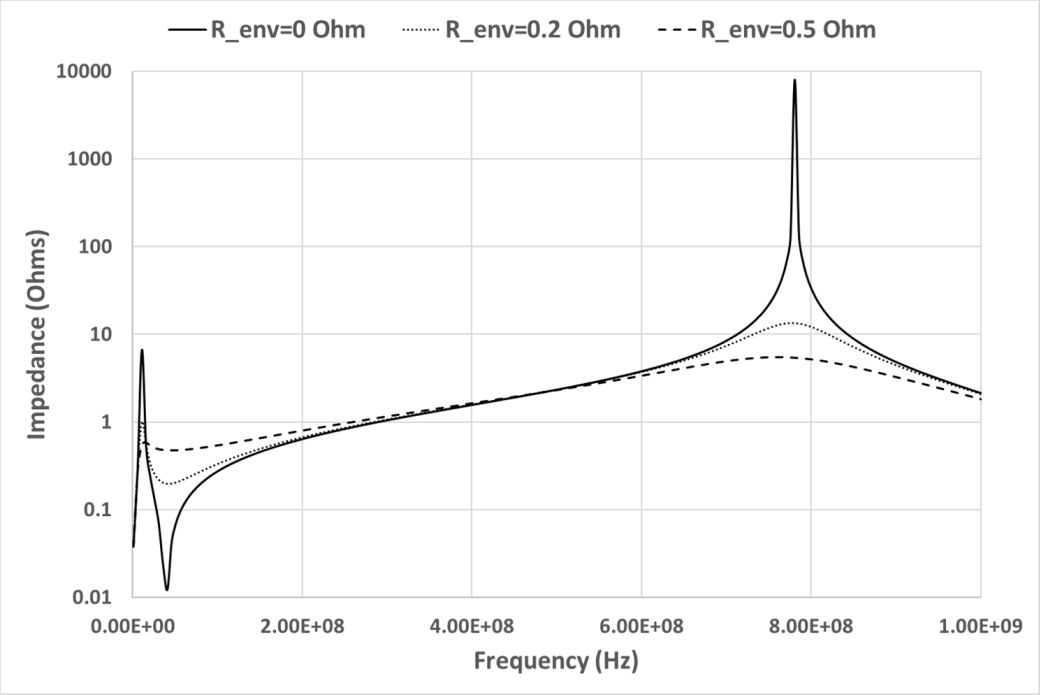

Figure 26: Magnitude of the Impedance presented to the Drain of the MOSFET by the network of Figure 25 [19]

IM3 can then be plotted as a ratio of H_3 to H_1 as per Eq. (25), as shown in Figure 27. It can be seen that the peak value of IM3 can be reduced by the presence of a damping resistor. The value of this resistor is to be chosen in order to obtain critical damping for the RLC circuit. This is discussed in detail in section 4.8.4.

The object of the proposed research is to improve the Video-Bandwidth Capability of RF Power Transistors by modifying the resonant behavior of the gate and drain envelope terminations.

4.3 Improvement in the Drain Baseband Resonant Frequency

Figure 28 shows a schematic of the proposed methodology for Video-Bandwidth Improvement. It consists of series R-L-C network connected to the node between inductor L_1 and Capacitor C_1. The values for these components are selected based on the

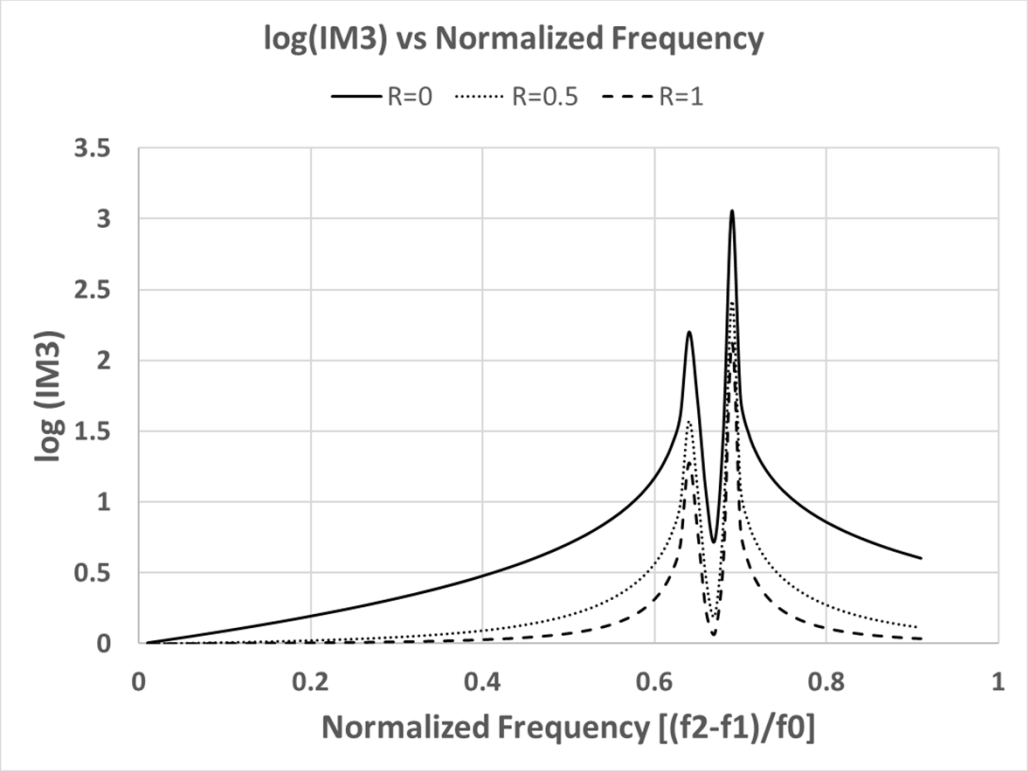

Figure 27: IM3 as a function of normalized delta frequency with Damping Resistor R [19]

following:

- Inductance L_3: The value of this inductance should be small so as to increase the resonance frequency of the baseband network to very high frequencies. A typical value would be 0.3 nH and can be realized using wirebonds. This component should also provide a high impedance at the fundamental frequency of operation so as not to load the fundamental match for the RF Power Transistor.

- Resistor R_1: The purpose of this resistor is to damp the self resonant frequency of the series R-L-C network. Its value is chosen to be 0.5 Ohm for this application.

- Capacitor C_3: Functionally, this capacitor is used as a decoupling component.

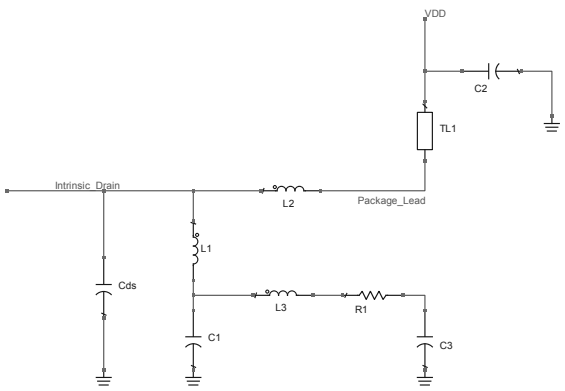

Figure 28: Drain Side Video-Bandwidth Enhancement

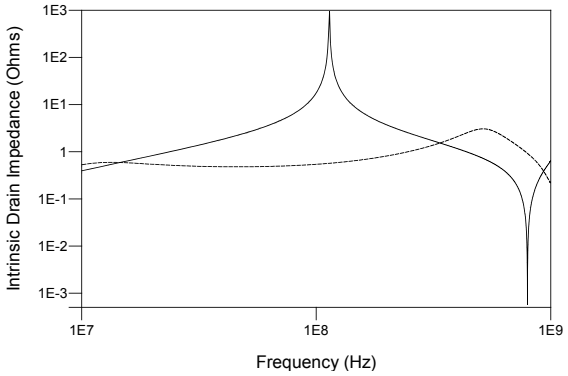

Figure 29: Impedance Presented to the Intrinsic Drain of the FET as a function of Frequency with and without the decoupling network

Table 4: Component Values for Figure 28

Schematic Component	Value
Cds	24pF
C1	120pF
C2	1uF
C3	82nF
L1	0.25nH
L2	0.2nH
L3	0.3nH
R1	0.5Ohm
TL1	Quarter-Wave at Fundamental Frequency

As a result, its value is chosen to be in the nF or μF range.

Figure 29 shows the intrinsic drain impedance response vs frequency for the cases with and without the decoupling network. As can be seen, the self bias resonance frequency has been increased from 114MHz to 533MHz and the magnitude of the impedance has also been significantly reduced in the entire baseband region. Table 4 shows component values used for simulation.

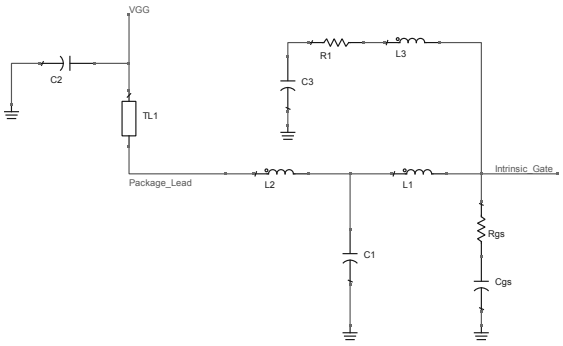

Figure 30: Gate Side Video-Bandwidth Enhancement

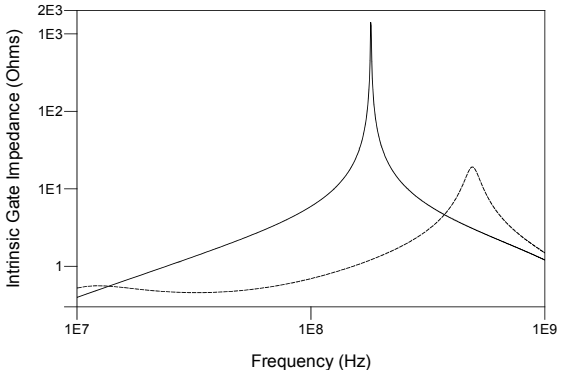

Figure 31: Impedance Presented to the Intrinsic Gate of the FET as a function of Frequency with and without the decoupling network

4.4 Improvement in the Gate Baseband Resonant Frequency

Figure 30 shows a schematic resulting from applying the proposed methodology for Video-Bandwidth Improvement on the Gate Side of the FET. Similar to the drain side case, we connect a series R-L-C network at the gate terminal of the FET. The component selection criteria is similar to the previous case with drain bias.

Figure 31 shows the intrinsic gate impedance response vs frequency for the cases with and without the decoupling network. As can be seen, the self bias resonance frequency has been increased from 180MHz to 488MHz and the magnitude of the impedance has also been significantly reduced in the entire baseband region.

It has been observed experimentally that for large periphery devices, where the gate to source capacitance can be several hundred pF, the gate baseband resonance can be quite low (observed by the author). In these cases, its important to dampen or shift the resonance higher in frequency using a gate bias IBN because the amplifier can have impaired stability or even poor linearity and predistortion performance.

4.5 Class AB power Amplifier with Enhanced Video-Bandwidth RF Power Transistor

The above drain side enhancements were applied to a Class AB application using a 140W (P1dB) LDMOS RF Power Transistor operating between 2.11-2.17GHz [22]. Figure 32 shows the two tone response at a constant output power for a standard device. Figure 33 shows the two tone response for a video-bandwidth enhanced device at constant output power. It can be seen the Video-Bandwidth has been improved from approximately 50MHz to greater than 100MHz from the perspective of the IM3 product. The technique also shows dramatic improvements in the fifth and seventh order IMD products (IM5 and IM7).

The importance of the damping resistor was proved experimentally using the above 140W Class AB Power Amplifier. The input signal used was a 2-Carrier WCDMA (10MHz) configuration. The bottom plot of Fig.34 shows correction with a baseband termination with a damping resistor. Here the correction level is close to the system's noise floor at -60dBc. The plot at the top shows the case of no damping resistor used. It can be seen that the correction is limited and this is attributed to the secondary resonance introduced by the integrated baseband termination LC network.

Considering H_3 at $(2\omega_2 - \omega_1)$ & $(2\omega_1 - \omega_2)$:

$$H_3(j\omega_1, j\omega_1, -j\omega_2) = \frac{-\beta(2\omega_1 - \omega_1)L}{1 - (2\omega_1 - \omega_2)^2 LC} f_1(H_2) \tag{36}$$

$$H_3(j\omega_2, j\omega_2, -j\omega_1) = \frac{-\beta(2\omega_2 - \omega_1)L}{1 - (2\omega_2 - \omega_1)^2 LC} f_2(H_2) \tag{37}$$

where f_1 and f_2 are functions of the second order volterra kernel H_2 as described in [16] by Pedro et al.

$$H_2(-j\omega_1, j\omega_2) = \frac{3V_T\beta(\omega_2 - \omega_1)L}{1 - (\omega_2 - \omega_1)^2 LC} \tag{38}$$

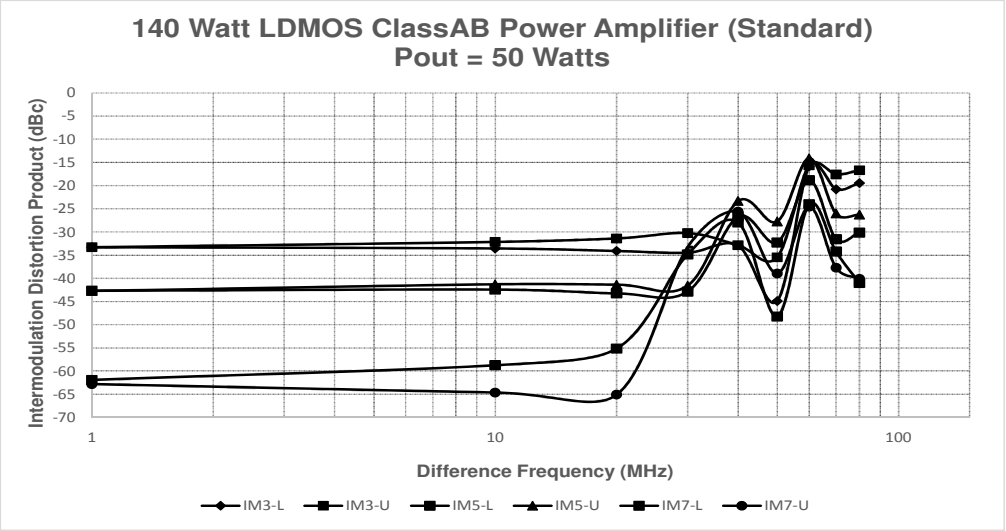

Figure 32: Two-Tone Test for Class AB Power Amplifier with Standard LDMOS Power Transistor

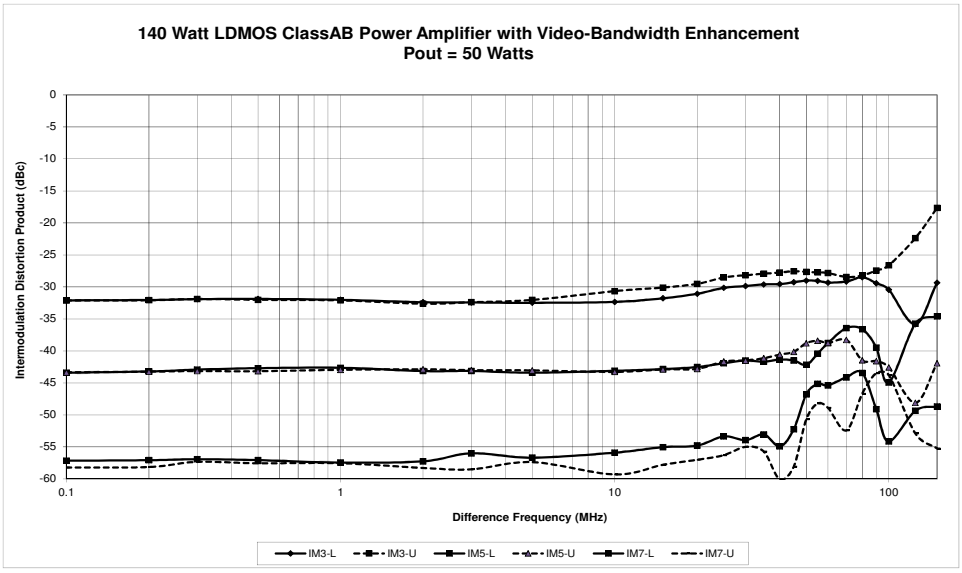

Figure 33: Two-Tone Test for Class AB Power Amplifier with Video-Bandwidth Enhanced LDMOS Power Transistor

This term is a function of the difference frequency and its presence in the H_3 equation shows the dependence of H_3 on and thus IMD_3 on $(\omega_2 - \omega_1)$. The magnitude

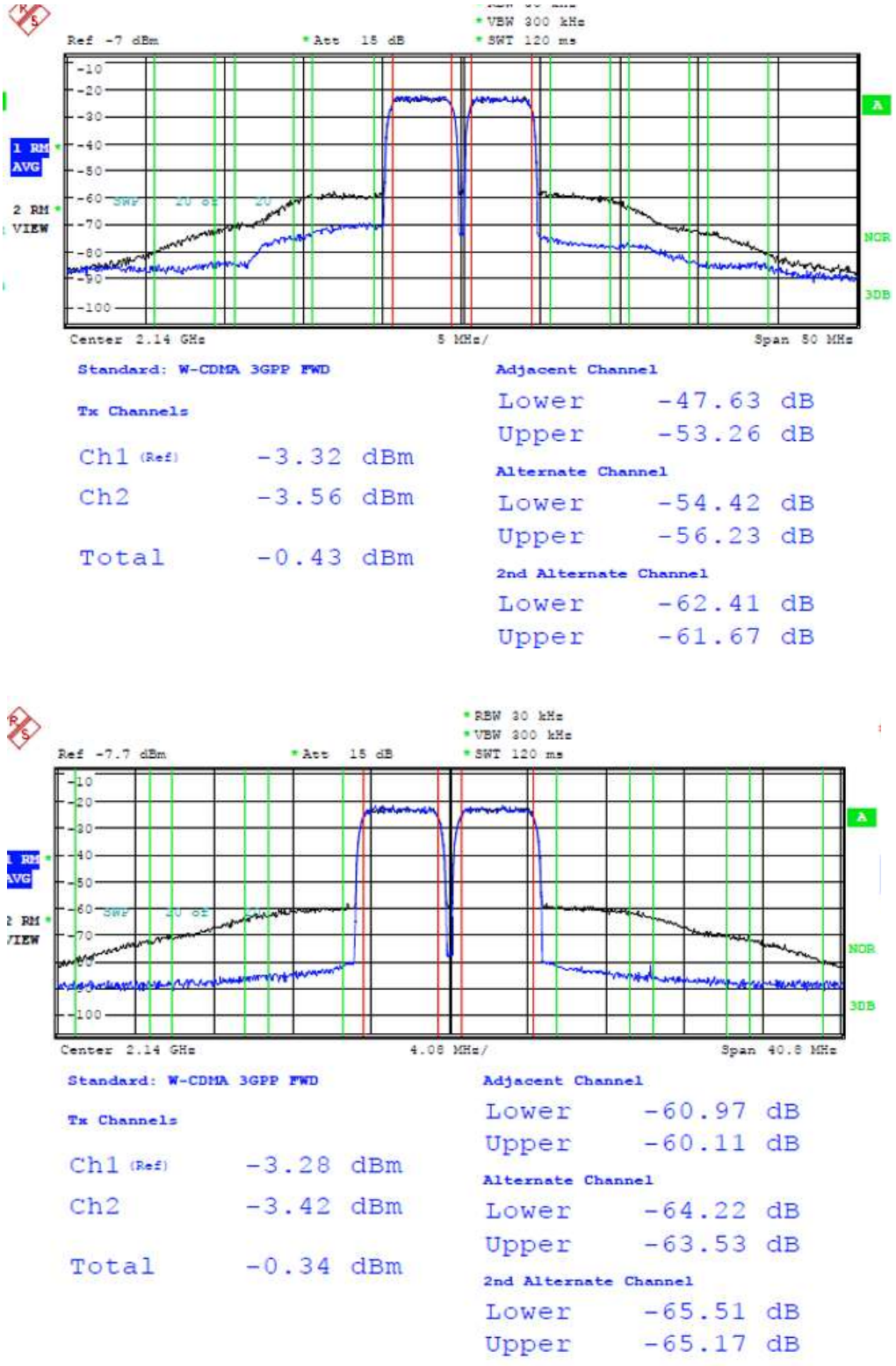

Figure 34: DPD Plots showing the impact of drain bias damping resistor. Without damping (top) and and with damping (bottom)[19]

of the H_2 term depends on the values of L & C. Thus it can be concluded that through H_2 , some of the asymmetry in the H_3 kernels can be attributed to the reactive components in the baseband through the H_2 kernel.

The intermodulation product at the difference frequency can be written as:

$$IM_2 = \frac{H_2(j\omega_1, -j\omega_2)}{H_1(j\omega_1)} \tag{39}$$

$$IM_2 = \frac{-1}{V_T}\frac{R + j(\omega_1 - \omega_2)L}{R + j\omega_1 L}.\frac{1 - \omega_1^2 LC}{1 - (\omega_1 - \omega_2)^2 LC} \tag{40}$$

The H_2 kernel and IMD_2 have a different response to the damping resistor than the H_3 kernel and IMD_3. From simulations, its magnitude actually increases with increasing R for the H_2. Since we are looking at H_2 and IMD_2 at the difference frequency ($\omega_2 - \omega_1$), by adding a resistor we are actually raising the baseband impedance (although it is very small at 0.5 to 1 Ohm). This explains why H_2/IMD_2 increases. From Pedro et al, the asymmetry in IMD3 is a function of the reactive portion of the difference frequency impedance. Lowering the value of the inductance (for example), the H_2/IMD_2 resonance actually moves up in frequency, since we are reducing the reactance at baseband.

4.6 Symmetric Doherty power Amplifier with Enhanced Video-Bandwidth RF Power Transistor

The above drain side enhancements were applied to a Symmetric Doherty Amplifier in the 1930-1995MHz frequency band [23]. Figure 35 shows the lineary and efficiency performance under various signal bandwidths over output power. Figure 36 shows the spectrum plot for the PA performance under 65MHz of composite signal bandwidth with DPD applied.

Signal bandwidth	Pout [dBm]	Eff. [%]	ACPR after linearization [dBc]			
			Lower end of band (3xCDMA)		Upper end of band (1x LTE)	
			ACPR L	ACPR U	ACPR L	ACPR U
40MHz	45.0	42.4	-69.07	-70.48	-58.89	-58.16
	45.8	44.6	-65.28	-66.90	-52.90	-52.83
	46.3	45.8	-61.61	-63.92	-48.54	-48.49
65MHz	45.4	43.2	-68.85	-68.55	-56.67	-53.12
	45.8	44.3	-64.56	-66.76	-52.57	-50.56
	46.2	45.5	-62.77	-65.46	-49.80	-47.77
80MHz	44.2	41.3	-70.83	-70.36	-58.41	-55.34
	45.2	42.6	-68.93	-66.26	-54.98	-50.47
	45.6	43.6	-67.05	-65.07	-52.58	-47.33

Figure 35: Digital PreDistortion Results for Symmetrical Doherty With Enhanced Video-Bandwidth LDMOS Power Transistor [23]

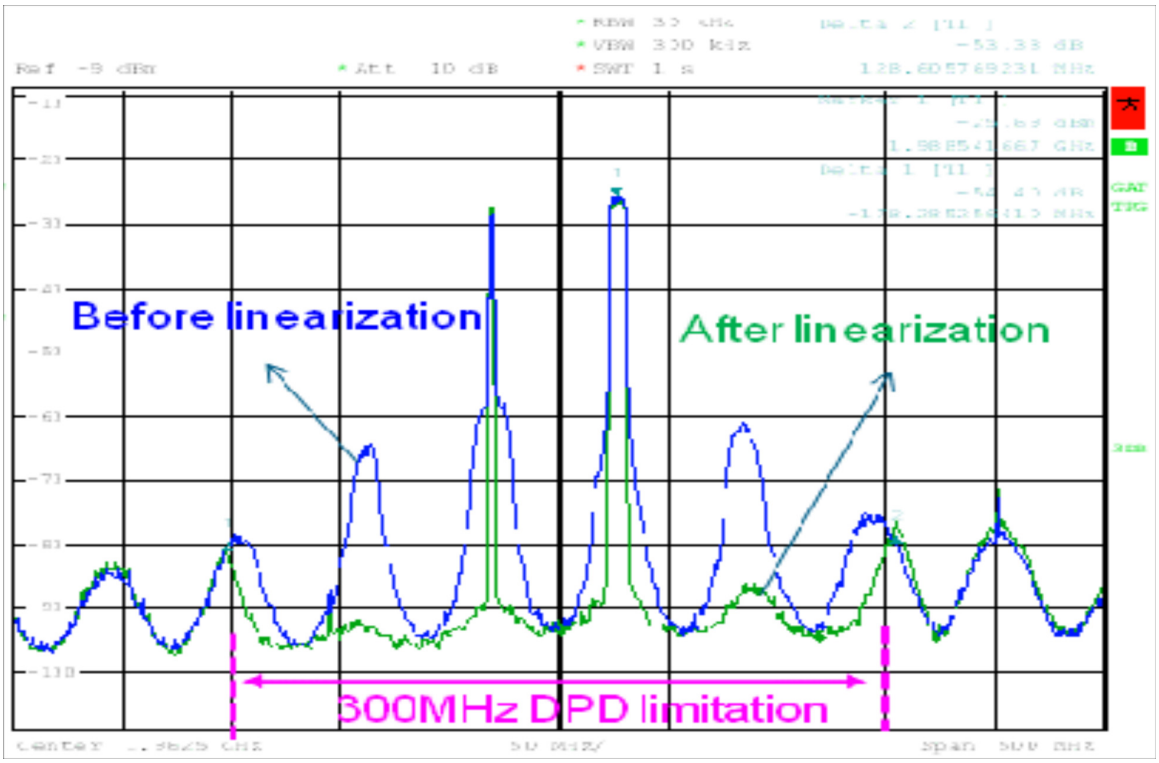

Figure 36: Spectrum Plot showing Pre and Post DPD Results for Symmetrical Doherty With Enhanced Video-Bandwidth LDMOS Power Transistor [23]

4.7 2-Way Asymmetric Doherty With Integrated Baseband Network

Figure 37 shows a block diagram of a 2-way Doherty power amplifier with an integrated baseband termination network. Figure 38 shows the circuit schematic of how

this network is implemented inside a packaged Doherty Device. Resistors R_{env1} and R_{env2}, Inductors L_{env1} and L_{env2} and Capacitance C_{env} form the integrated baseband termination. This is connected to the node between Inductor Lshunt1 and Capacitor CBlock1 for the Carrier Amplifier and the node between Inductor Lshunt2 and Capacitor CBlock2 for the peaking amplifier. This connection allows the carrier and peaking paths to share the Integrated Baseband Network at DC and low frequencies. C_{env} performs the decoupling. L_{env1} and L_{env2} isolate the IBN from the carrier and peaking paths at the fundamental frequency, while R_{env1} and R_{env2} perform damping of the resonances present in this network. CBlock1 and CBlock2 are RF matching elements. The distortion generated at the intrinsic current sources are dependent on the envelope impedances presented by the IBN and external bias networks. However, no Doherty load modulation occurs at low frequencies and the IBN is isolated from the sub-amplifiers at the fundamental frequency by design. Due to the asymmetric nature of the carrier and peaking path amplifiers, the component values need to be specifically designed separately for them. Section 4.8.4 discusses the design of this network in detail. Figure 39 shows the assembly of a 400W power transistor with an Integrated Baseband Termination.

4.8 Doherty Design Procedure

This section will demonstrate the design methodology of a 400W peak Doherty Power Amplifier with an asymmetry ratio of 1.67 [33]. The operation of a Doherty Power amplifier can be summarized as follows: during low RF input power levels, the Peaking sub-amplifier with a Class C bias is effectively off and is practically disconnected from the load due to the high impedance seen into its output at the combining node. At high input drive levels, both amplifiers work together to provide their full power output capability. The operating impedances are chosen to allow for maximum power transfer into the load at full power. The Doherty Action occurs on the Carrier

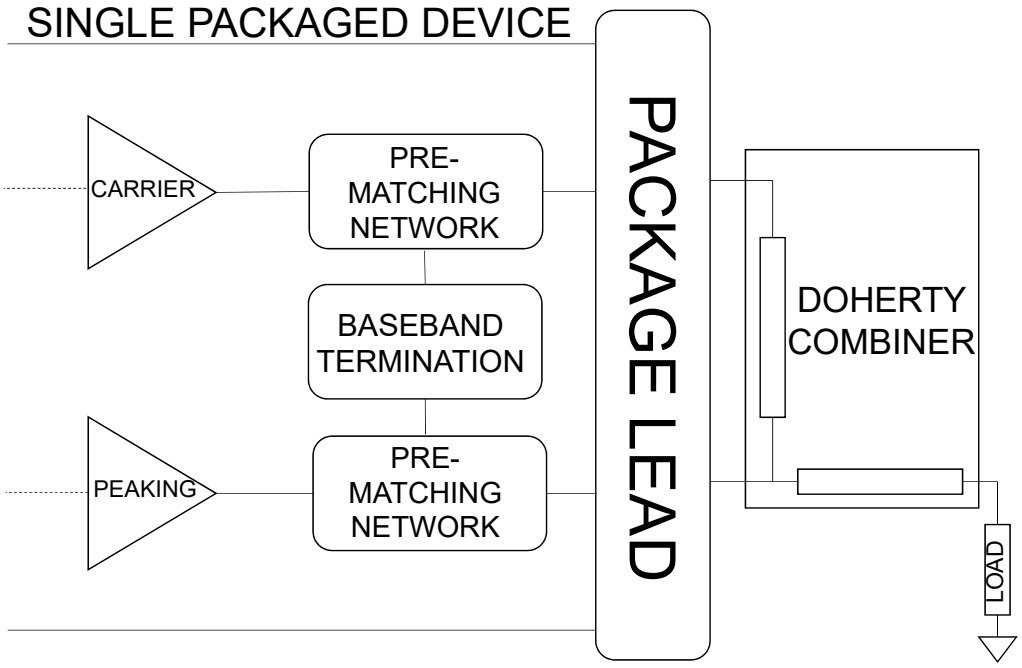

Figure 37: Block Diagram of an in-package Asymmetric Doherty Power Amplifier with Integrated Baseband Terminations

Amplifier as the input drive level is increased and the Peaking contributes power to the output. The Carrier Amplifier's load is designed to modulate between the high efficiency impedance when the Peaking Amplifier is off and its high power impedance when the Peaking Amplifier is on [10], [33].

4.8.1 Device Choice

For maximum efficiency at certain Output Back off, we use the below equation to size the devices.

$$B = 20log(r + 1) \tag{41}$$

where B = Backoff Level and r = Peaking to Carrier Power Ratio. Setting B = 8.5, the power ratio between the carrier and peaking device needs to be at 1.67

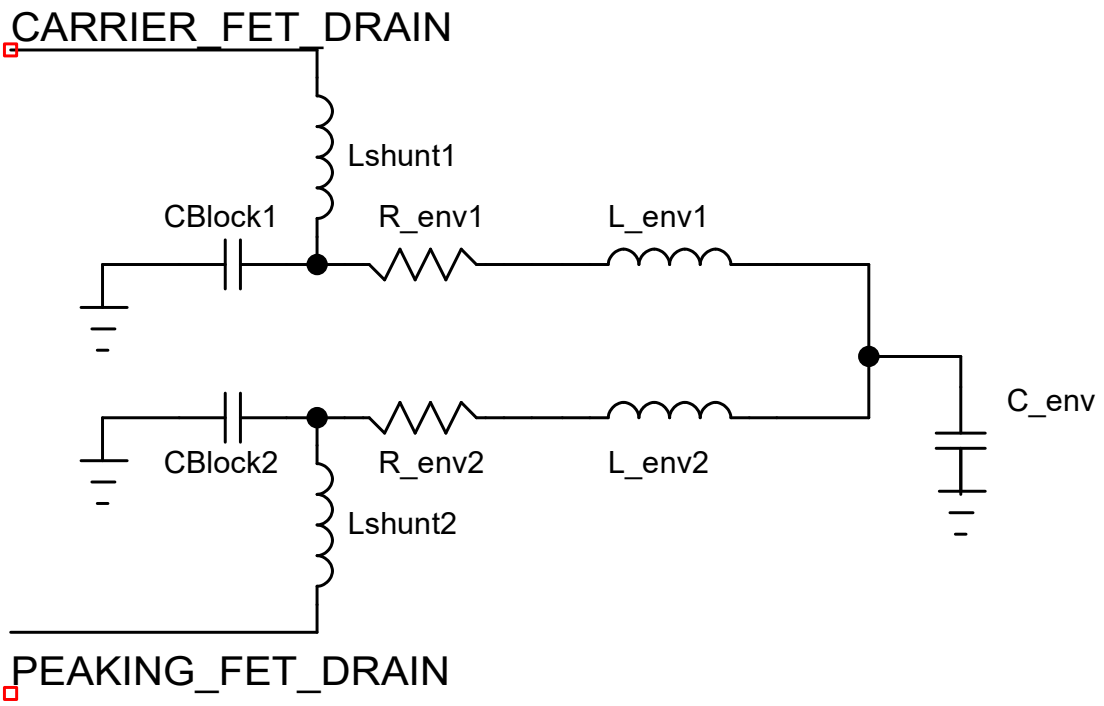

Figure 38: Schematic of the in-package Doherty Power Amplifier with an integrated Baseband Termination[33]

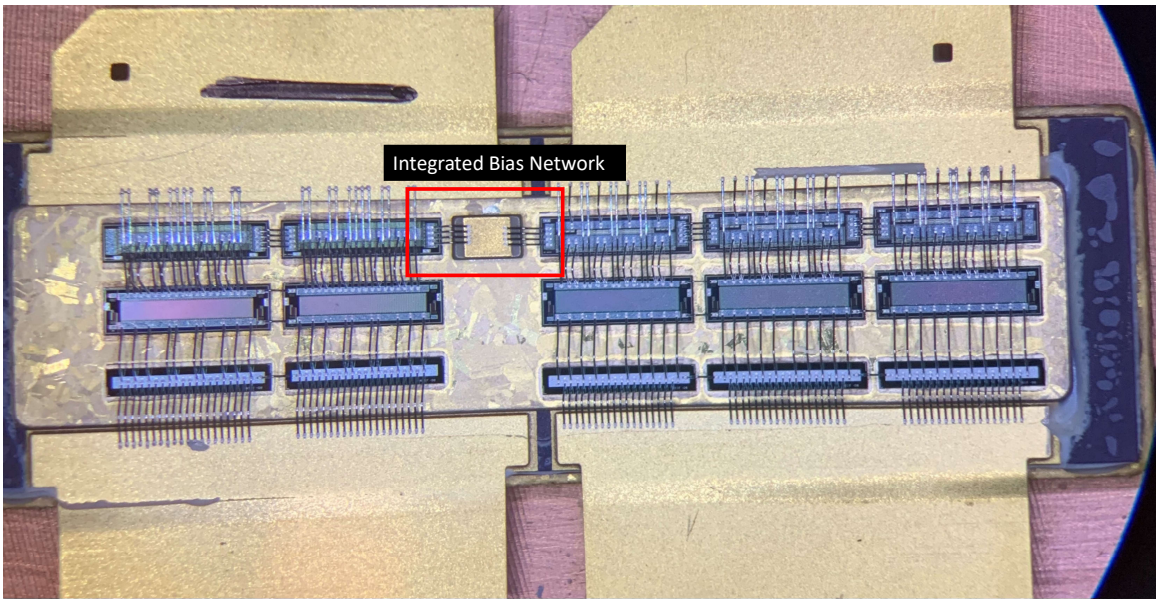

Figure 39: Image showing the assembly of the Asymmetric Doherty Power Transistor with a drain Integrated Baseband Termination[33]

$$\frac{P_{peak}(W)}{P_{carrier}(W)} = 1.67 \tag{42}$$

In our case, the design uses

$$P_{sat}(Carrier) = 150W \tag{43}$$

$$P_{sat}(Peaking) = 250W \tag{44}$$

For a two-way Doherty, both the carrier and peaking devices could be designed separtely in their own packages. Following the industry trend to reduce PCB area, it is of great value to design both carrier and peaking devices inside a single package for size, cost and performance benefits (mainly due to higher integration of matching networks).

The carrier and peaking devices are typically designed separately to optimize the performance for their mode of operation. The carrier amplifier should provide high gain and high efficiency at the required backoff as well as low impedance dispersion at the device terminals. The peaking amplifier should have a high off state impedance and fast turn on time.

4.8.2 Doherty Combiner Design

Figure 40 shows the components of a Doherty Combiner.

For a given Power ratio:

$$r = \frac{P_{peak}(W)}{P_{carrier}(W)} = 1.67 \tag{45}$$

We choose the carrier characteristic impedance Z_c to be

$$Z_c = 50\ \Omega \tag{46}$$

Then the combining impedance R_o is calculated as

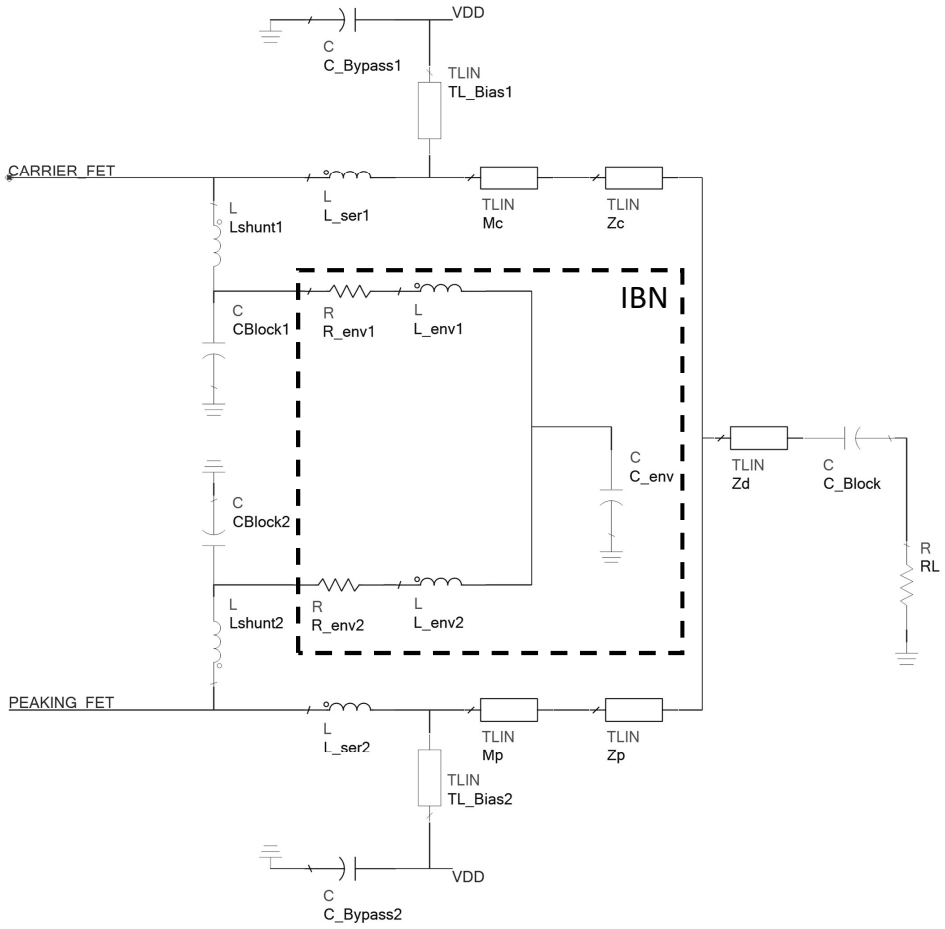

Figure 40: Circuit Schematic Showing the Design of the Proposed Doherty Combiner

$$R_o = \frac{Z_c}{1+r} = 18.7\ \Omega \tag{47}$$

The peaking characteristic impedance is calculated as

$$Z_p = R_o(1+\frac{1}{r}) = 29.9\ \Omega \tag{48}$$

The Doherty transformer characteristic impedance is calculated as

$$Z_d = \sqrt{R_o * R_L} = 30.6\ \Omega \tag{49}$$

The Class AB Carrier Amplifier Matching Circuit (Mc) simultaneously supports two load conditions : a high efficiency state when the peaking amplifier is off and a

high power state when the peaking amplifier is fully conducting. The high efficiency tuning is accomplished with the connection to the R_o node without the peaking amplifier connected. This will produce an impedance of 135 Ohm (50 Ohm x 2.7) at the combining node. The high power tuning is accomplished with the load set to 50 Ohms and can be accomplished with a separate 50 Ohm line connecting to the output of TLIN Mc.

The Class C Peaking Amplifier matching circuit (TLIN Mp) simultaneously supports two load conditions : high power and high off-state impedance. The Peaking off-state phase length is simulated using Off-State S-Parameter measurements de-embedded to the output S22 at device plance. The phase line Z_p is designed to provide a high impedance at the combining node under low power conditions. The efficiency degradation of the carrier amplifier in the low power state should be kept low by proper design of the off-state network.

Table 5 shows transmission line impedances and electrical lengths for the elements of the Doherty network.

Table 5: Transmission Line Impedances and Electrical Lengths for Figure 40

Schematic Element	Characteristic Impedance	Length at 1842.5MHz
Mc	6.956 Ω	58.4 °
Zc	50 Ω	168.8 °
Mp	7.729 Ω	60.3 °
Zp	29.9 Ω	102 °
Zd	30.6 Ω	90 °
TLBias1	28.1 Ω	90 °
TLBias2	28.1 Ω	90 °

4.8.3 Input Splitter

The main function of an input splitter is to divide the input power between the carrier and peaking paths. The split ratio between the paths will determine the gain response of the Doherty PA and can have an appreciable impact to the overall linearity of the Doherty circuit. In this application, we use an equal split branch line coupler[34].

Figures 41, 42 and 43 show measured responses of the power splitting network.

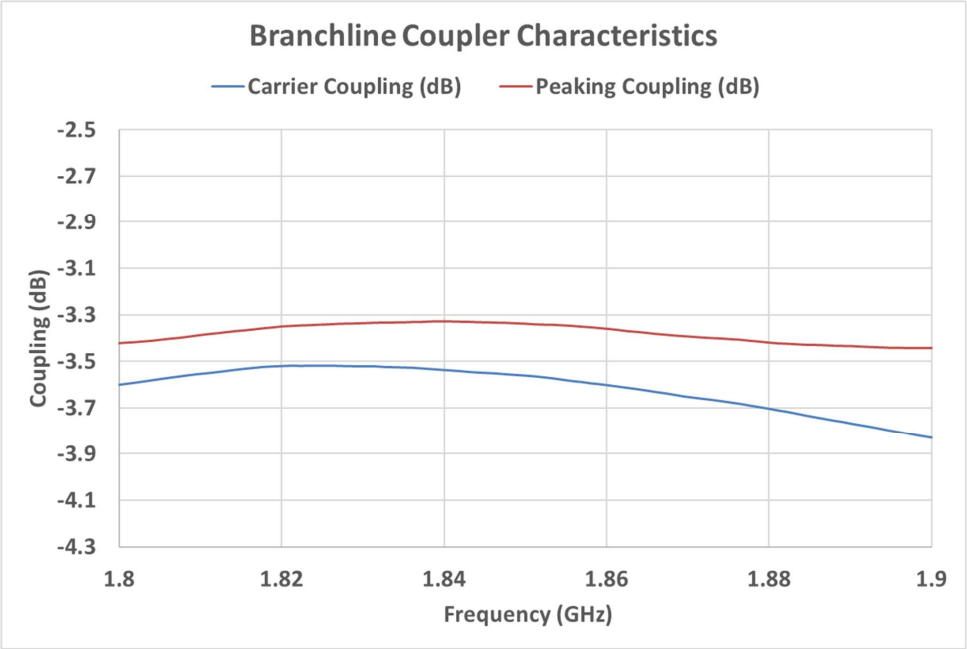

Figure 41: Input Splitter Coupling Characteristics

4.8.4 Design of Integrated Bias Network

The primary purpose of the Integrated Bias Network (IBN) is to enhance the Video-Bandwidth capability of the RF power transistor. In our application, the IBN is shared between the Carrier and Peaking PAs. The component values are selected such that at the frequency of operation, both amplifiers are isolated by presenting a high impedance to each other. The following sections discuss the design and technology considerations of this network.

4.8.4.1 Envelope Capacitor (C_env)

The envelope capacitor's main function is to present a low impedance to the intrinsic drain of the FET in the baseband frequency region. As such, it is a high value capacitor and is usually composed of a dielectric made up of a ferroelectric material such as Barium Titanate. The design of the capacitor has to be undertaken satisfying

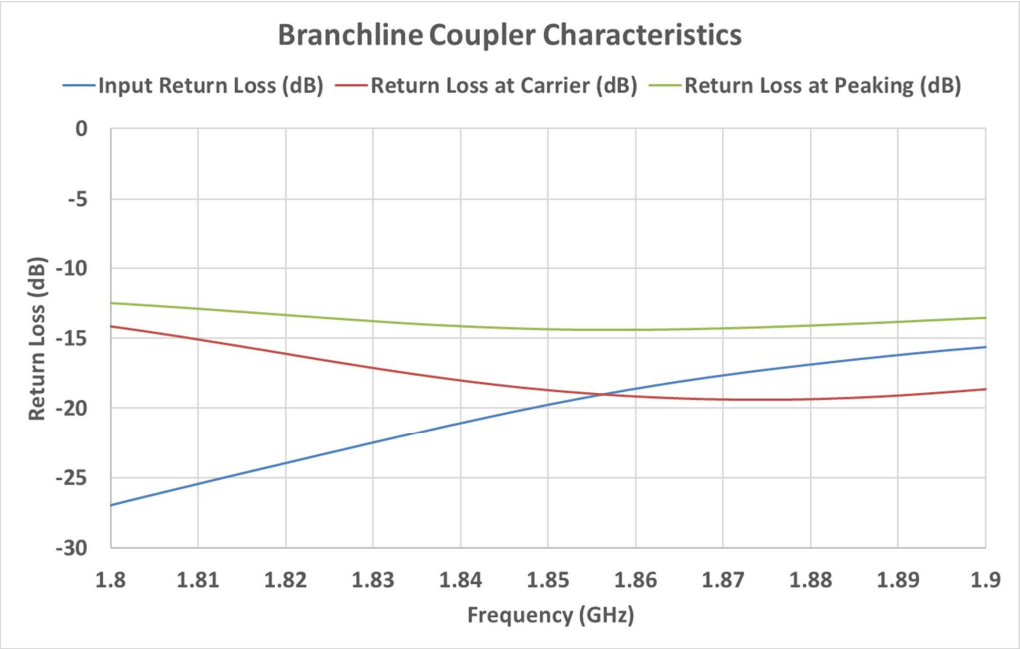

Figure 42: Input Splitter Return Loss Characteristics

several parameters that limit how high of a capacitance can be achieved. Some of these are :

Breakdown Voltage The capacitor is designed to have a breakdown voltage at least twice the DC voltage applied to the capacitor. (For example, for a 28V application, this would be > 56V)

Dielectric Temperature Characteristics Typical RF Power transistors are used in applications that require operation between -55 to +125C. The capacitor's dielectric must be stable over this temperature range. X7R or X5S dielectrics exhibit this characteristic.

Capacitance For a given part size, the capacitance is maximized by controlling the number of parallel plates that form the electrodes, plate area as well as the distance

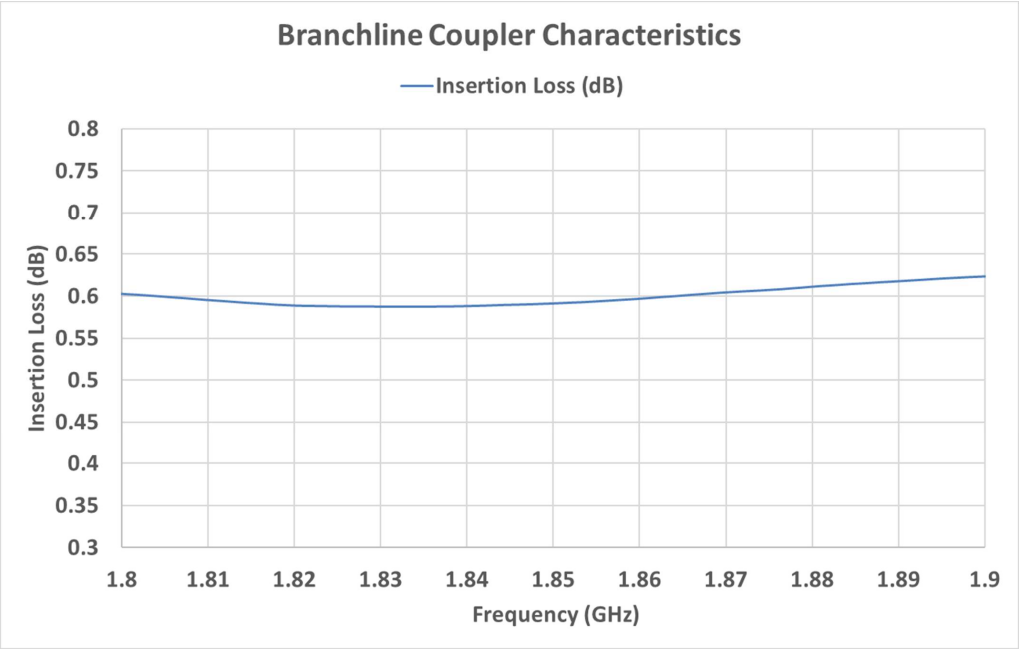

Figure 43: Input Splitter Insertion Loss Characteristics

between the plates.

$$C = \epsilon * Area/d \tag{50}$$

For high value dielectrics, the capacitance typically reduces as a function of applied DC voltage. For this application, the 0V Capacitance is 82nF and its 28V value is 30 nF.

Assembly The capacitor surface is to be wirebondable. Thus, its termination is an alloy consisting of Cu/Ni/Au plating that allows for Aluminum wire bonding .This plating also allows soldering to the package flange.

4.8.4.2 Envelope Inductor (L_env)

The purpose of the envelope inductor is to isolate the Integrated Bias Network from the RF matching circuit. The IBN is connected to the node between the matching

inductor (Lshunt) and the matching capacitor (CBlock). At this node, current division will take place depending on the level of the relative impedance of both paths. In this application, L_env is realized using aluminum wirebonds.

We can define an impedance ratio :

$$A = \frac{X\_Lenv}{X\_CBlock} \tag{51}$$

where X_Lenv and X_Cblock are defined as:

$$X\_Lenv = 2\pi(freq)(L\_env) \tag{52}$$

$$X\_CBlock = \frac{1}{2\pi(freq)(C\_Block)} \tag{53}$$

By assigning a sufficiently high value to A, we can derive the value of the inductance required for L_env. It was found through simulations that A>10 provides sufficient isolation for the IBN such that the fundamental frequency current leakage into the IBN is minimized. As an example, for circuit operation at 1845 MHz, for CBlock=240pF (DC Blocking) and A=10 gives an L_env value of 0.3nH. At lower frequencies, this value will be larger for good isolation.

4.8.4.3 Envelope Resistor (R_env)

The envelope resistor's primary function is the dampen the very low frequency resonance present in the interaction between the IBN and the prematching and external bias circuits. Assuming the entire network can be simplified to a parallel RLC circuit, we can define two parameters : Resonant Frequency ω_0 and Neper Frequency α :

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{54}$$

$$\delta = \frac{1}{2RC} \tag{55}$$

A parallel resonant circuit is

Overdamped If $\delta > \omega_0$

Underdamped If $\delta < \omega_0$

Critically damped If $\delta = \omega_0$

In our application, we would like the IBN network along with the rest of the circuit to be critically damped, so that it doesn't present any resonances to the intrinsic current source (underdamped) as well as it does not increase losses due to an excessive power drop at envelope frequencies (overdamped). Thus equating δ to ω_0, we can determine the value of R that results in a critically damped system. In our circuit, L=0.3nH, C=240pF, results in an R value of 0.5 Ohms.

The resistor R_env will dissipate some power at the envelope frequencies. Thus it is necessary to simulate the power drop across it using a two tone test at the intended operating power level. To improve power handling capability, multiple resistor segments are connected in parallel. The resistor segments are formed using Tungsten Silicide material on a silicon substrate (same process as that used to form the LDMOS power transistor). Simulations show that under Doherty average power conditions and 75MHz of signal bandwidth, the rms current across the resistor is about 400mA (envelope current).

4.9 Doherty Performance

Figure 44 shows a photograph of the designed Doherty Circuit. It achives an 8 dB backoff efficiency of 50% in the DCS band with a gain > 15 dB and a peak output power of 400W. Figure 47 shows VNA Power Sweeps of the Doherty Circuit. The input signal PAR compression is at 2.5 to 3dB across 240MHz. Figure 46 shows a two tone plot demonstrating a resonance free IMD3 range > 200 MHz. For the

case with no IBN, the VBW is limited to 40 MHz. Table 6 summarizes the Doherty performance.

To demonstrate the capability of the baseband termination topology introduced earlier to real-world conditions, we performed DPD measurements using a standard multi-carrier test signal. Predistortion linearizers are commonly used to compensate for nonlinear distortion while maintaining reasonable PA power efficiency [35-42]. A predistorter basically introduces a nonlinear module that has inverse characteristics of PA nonlinearity between the signal source and the PA. As a result, the output signal of the cascade connection of a predistorter and a PA gives a more linear output, and reduces interference[43]. The predistortion measurements were supported by Optichron [44].

Figure 45 shows a spectrum plot with and without DPD. The signal used was a 65MHz instantaneous bandwidth multi-carrier signal with 3-CDMA Carriers at the low end of the band and 1-LTE Carrier (10MHz) at the upper end of the band. The DPD correction was at -68dBc (Offset=885 KHz, BW=30 KHz) for the low band edge and -52 dBc (Offset=10 MHz, BW=9.6 MHz) for the upper band edge.The signal was centered at 1.84 GHz. Table 7 summarizes previously published results in the same power and frequency range.

Table 6: Doherty PA Performance (1-Carrier WCDMA Signal)

Parameter	1805 MHz	1845 MHz	1880MHz
Peak Power	56 dBm	56 dBm	56 dBm
Average Power	48 dBm	48 dBm	48 dBm
Gain (dB)	15.4 dB	15.8 dB	15.6 dB
Drain Efficiency	49.5%	51%	50%
Video-Bandwidth	>200 MHz	>200MHz	>200MHz

Table 7: Comparisons With Other Work [33]

Ref.	Topology	Frequency	Pavg.	Eff.Avg	Peak Power.	Tech	IBN	VBW
[45]	2-way	1.8-2.2GHz	48.5dBm	40%	56dBm	LDMOS	Yes	395 MHz
[46]	3-way	1.9-2.2GHz	49.5dBm	40%	>57dBm	GaN	No	10 MHz
[47]	2-way	2.11-2.17GHz	48.7dBm	45%	56.7dBm	LDMOS	No	5 MHz
[48]	2-way	1.8-2.2GHz	49.3dBm	45-59%	56.6-57.3dBm	GaN	No	60 MHz
[49]	3-way	1.8-1.88GHz	50.5dBm	52%	59dBm	LDMOS	No	60 MHz
[50]	3-way	1.8-1.88GHz	49dBm	55%	57dBm	LDMOS	No	20 MHz
[51]	2-way	2.14GHz	48dBm	49.8%	56dBm	LDMOS	No	5 MHz
This Work	2-way	1.8-1.88GHz	48dBm	50%	56dBm	LDMOS	Yes	>200MHz

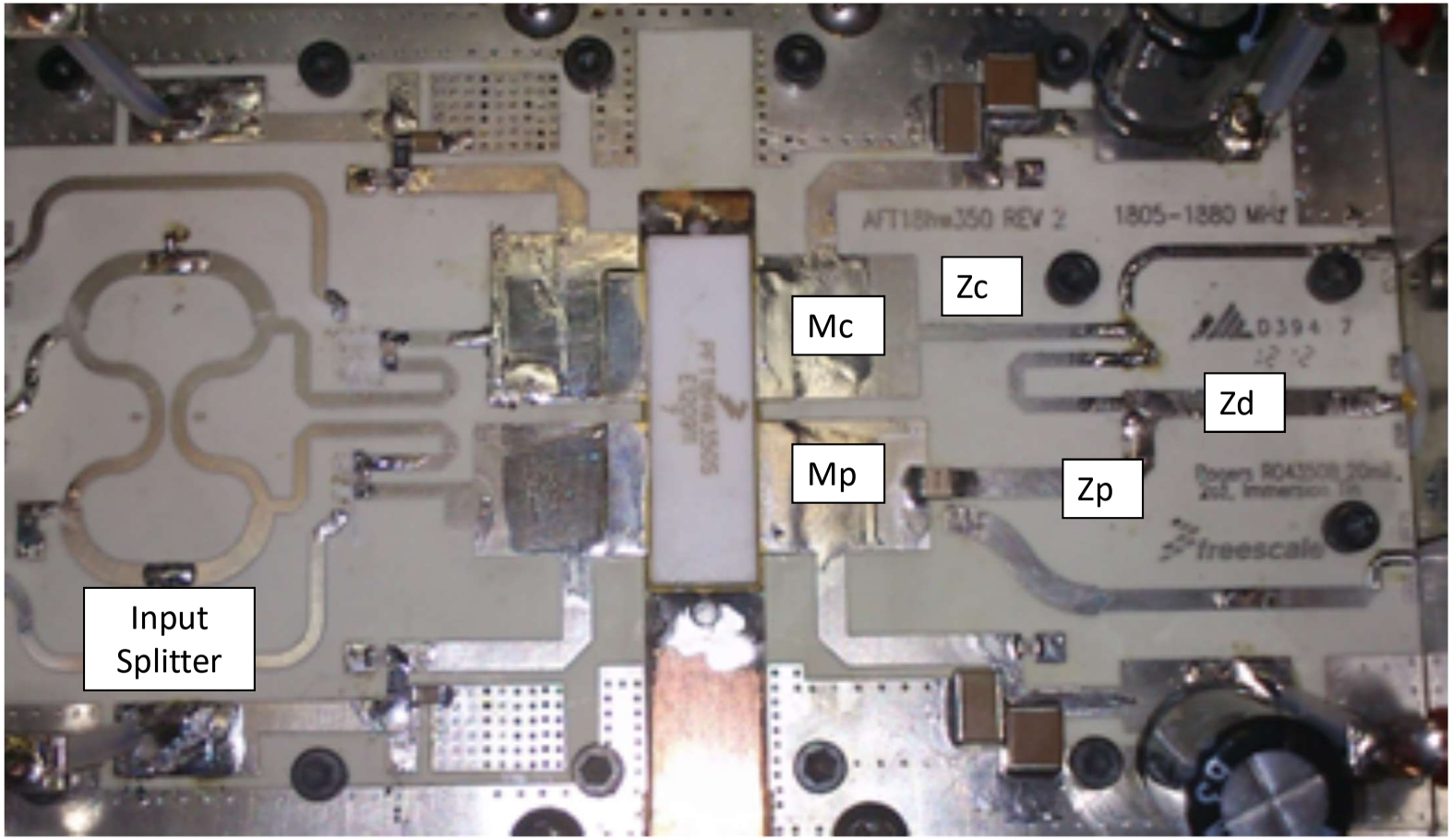

Figure 44: Image showing the built Asymmetric Doherty Power Amplifier with an in-package Doherty Device [33]

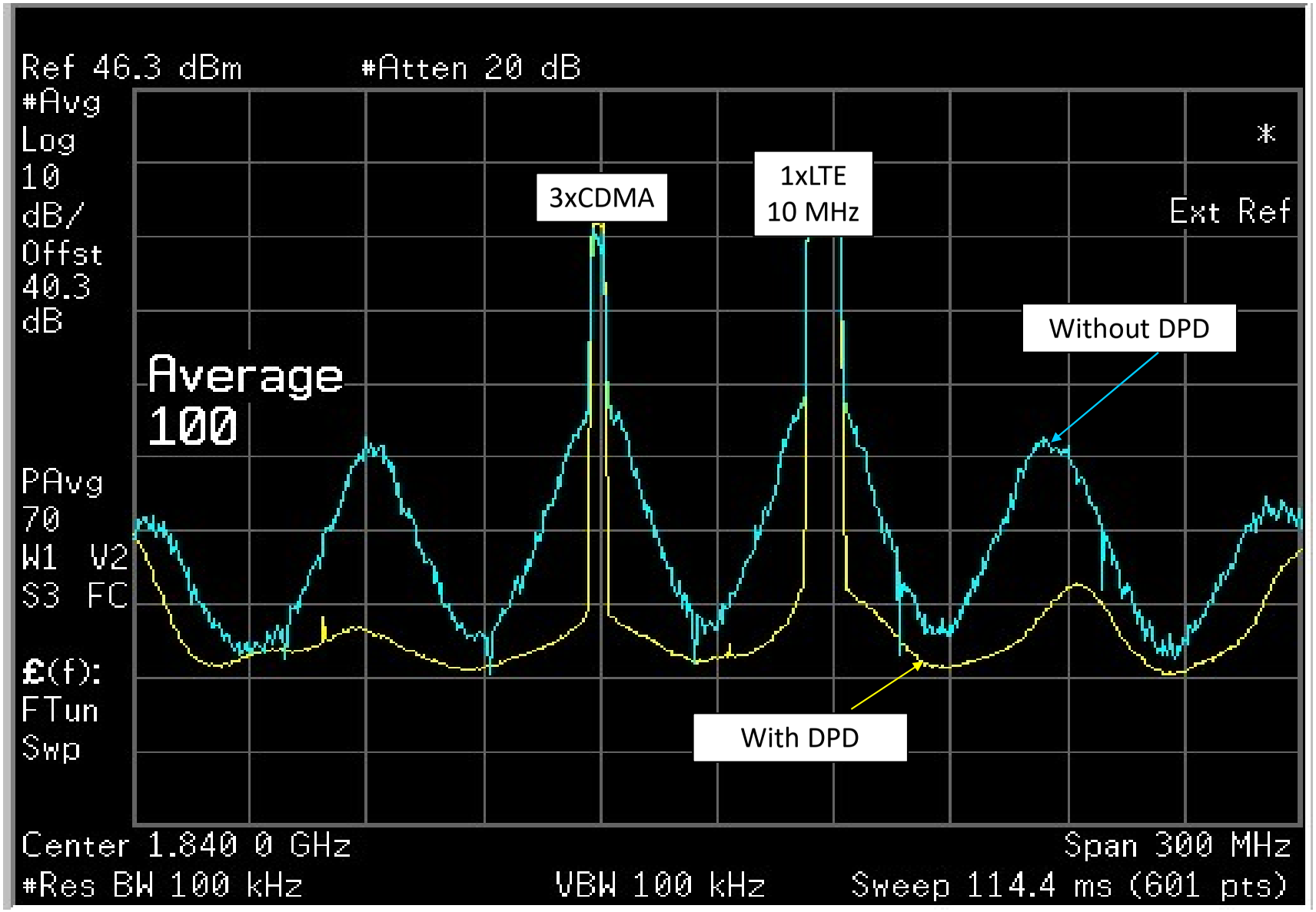

Figure 45: Digital Predistortion Spectrum Plot showing performance with and without correction to a 65MHz Multi-Carrier Multi-Standard Signal [33]

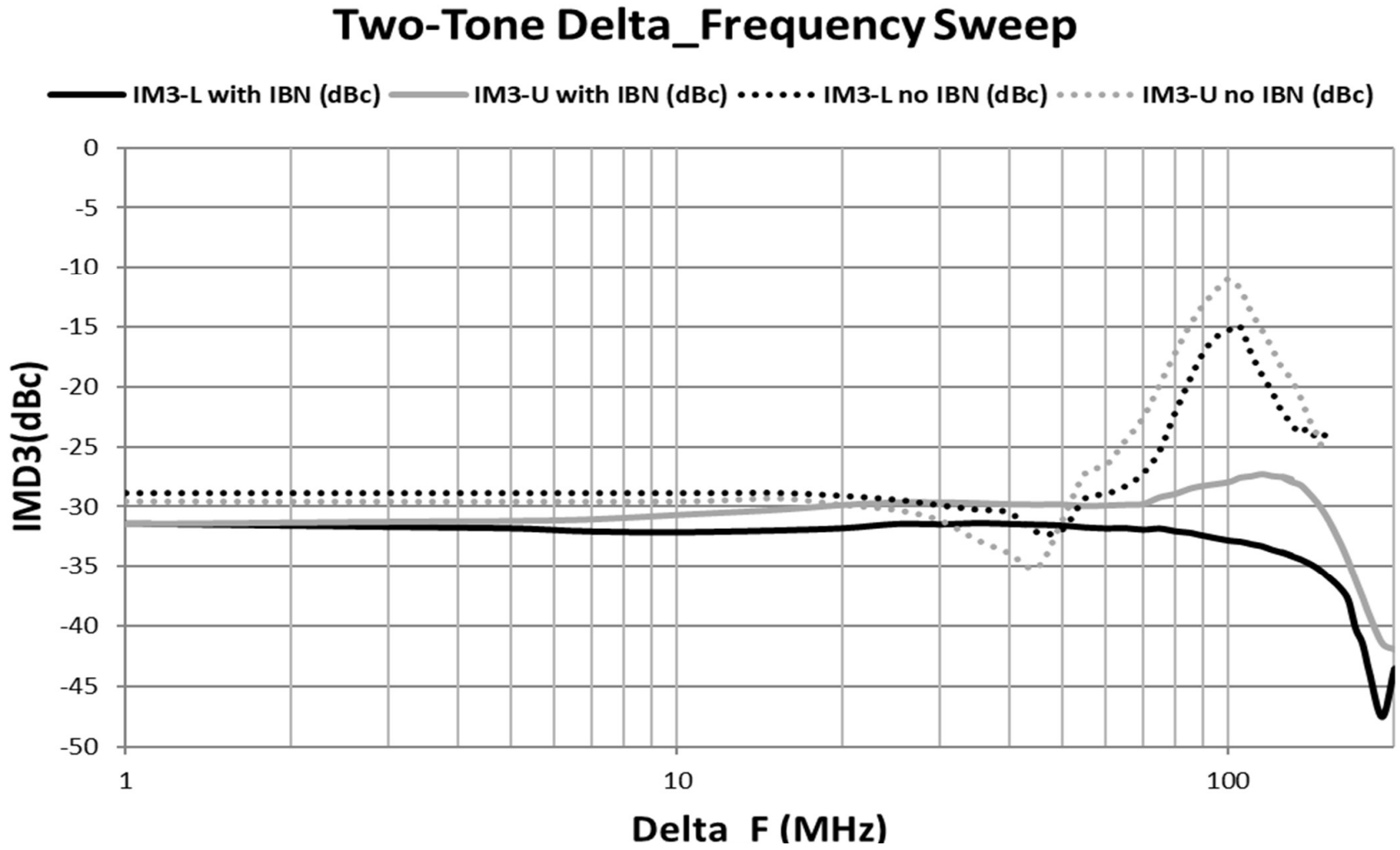

Figure 46: Two Tone plot demonstrating the enhanced video-bandwidth capability of the Asymmetric Doherty Power Transistor [33]

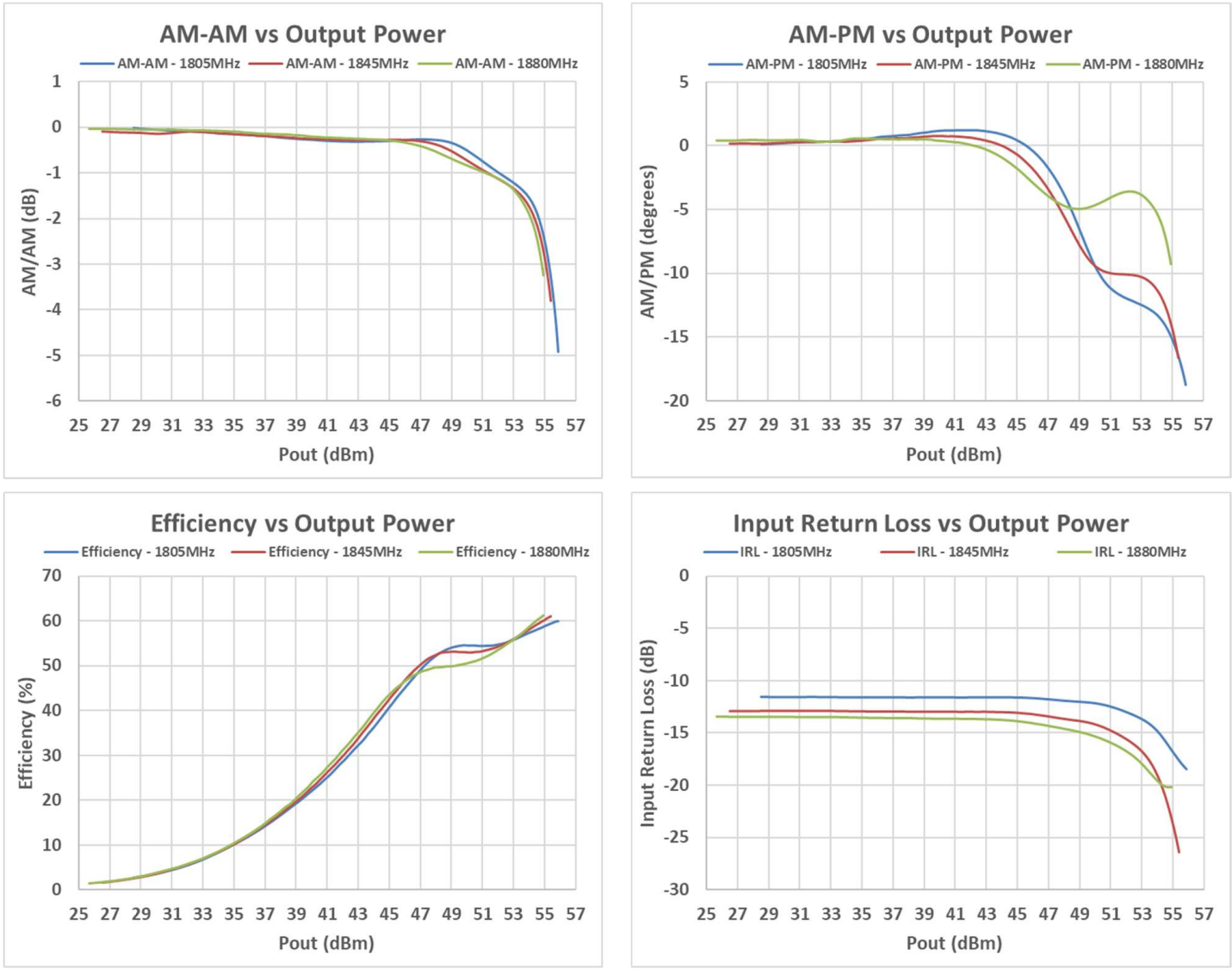

Figure 47: Doherty CW Performance (VNA Power Sweeps)

CHAPTER V

CONCLUSION

In this dissertation we derived Volterra Kernels for a CS Amplifier and discussed the limitations of RF power amplifiers with regards to low frequency envelope terminations. Equations were derived to show the variation of the baseband impedance across the modulation frequency range. A new topology was introduced and its efficacy was demonstrated with the low frequency resonance shifted much higher in frequency (outside the modulation frequency bandwidth). A damping resistor was shown to be necessary to address the very low and high frequency resonance that was introduced by this topology. We discussed the implementation of this IBN inside a packaged Doherty device and the performance achieved. Traditional efforts to improve VBW were limited to shortening the length of the power supply quarter wave line. Finally, an in-package Asymmetric Doherty was designed from 1.805-1.88GHz that incorporated this integrated baseband termination. The Doherty achieved an average efficiency of 50% at 8 dB OBO with good DPD correction for a 65MHz Multi-Carrier Signal. Table 7 shows a comparison of this work with other published results. [49] and [50] show higher efficiency than the current work, however the topology in both is a 3-way Doherty, their bias decoupling is external and the current work shows higher signal bandwidth DPD correction. For a 2-way Doherty, this work represents the highest efficiency reported for a power amplifier with an Integrated Bias Network. To the best of our knowledge, we believe that our results are the best achieved to date considering a combination of power output, efficiency and DPD correction bandwidth.

CHAPTER VI

FUTURE RESEARCH TOPICS

Although this research focuses on single stage high power PAs, video-bandwidth enhancement techniques can also be applied to multi-stage power amplifiers. This is of particular importance for mMIMO (Massive Multi-Input Multi-Output) systems, wherein two stage amplifiers are typically used for each of the carrier and peaking sub-amplifiers in a Doherty configuration. The impact of low frequency resonances from the first stage amplifier upon the performance of the lineup can be studied to assess if these resonances play a part in overall linearization performance, especially under very wide signal bandwidth conditions.

In this research, we apply a symmetric IBN network for both the carrier and peaking amplifiers. However, since these are biased in Class AB and Class C respectively, the envelope currents that result from Doherty operation may be different and this might suggest a different design for the IBN for both sub-amplifiers.

Since Gallium Nitride power transistors show power density roughly 10 times higher than LDMOS, a comparable GaN PA will be much smaller in periphery (higher output impedances) and may not require an output matching network. It needs to be studied whether an unmatched output GaN device would provide best video-bandwidth vs. a device that includes an output match with an IBN as discussed in this research.

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